Network of ICT
experienced organisations,
sharing experiences, knowledge
and supporting SMEs

Grant Agreement No.225004

# Join The Network

## 1 Embedded Systems

a. Starting up in Embedded System Design

b. Artist Design

c. Architecture Embedded Multimedia Applications

d. Foundations of Hybrid and Embedded Software and Systems

e. Embedded Systems - More

f. Home Automation and Embedded Devices

g. Trends and applications of embedded systems in Spain


**PROPOSAL/CONTRACT N.: 225004**

**PROJECT ACRONYM: NET-SHARE**

**PROJECT FULL TITLE: NETWORK OF ICT EXPERIENCED ORGANIZATIONS, SHARING EXPERIENCES, KNOWLEDGE AND SUPPORTING SME'S.**

**INSTRUMENT: ICT PSP**

**DURATION: 36 MONTHS**

**DISSEMINATION LEVEL: PUBLIC**

**PROJECT COORDINATOR ORGANISATION NAME:** Inovamais, S.A.; www.inovamais.pt

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**PARTNER NAME: INOVA+**

**CONTACT PERSON: MIGUEL SOUSA**

**GOOD PRACTICE NAME: STARTING UP IN EMBEDDED SYSTEM DESIGN**

**SOURCE OF THE GOOD PRACTICE: VAHID.GIVARDIS.COM**

**TARGET GROUP: SMES**

**DATE: 12 DECEMBER 2009**

Embedded Systems Design: A Unified Hardware/Software Introduction

# Starting up in Embedded Systems Design

# Outline

- Embedded systems overview
  - What are they?
- Design challenge – optimizing design metrics
- Technologies
  - Processor technologies
  - IC technologies
  - Design technologies

What are Embedded Systems? – An overview

Design challenge – optimizing design metrics

Technologies – Processor technologies
- IC technologies
- Design technologies

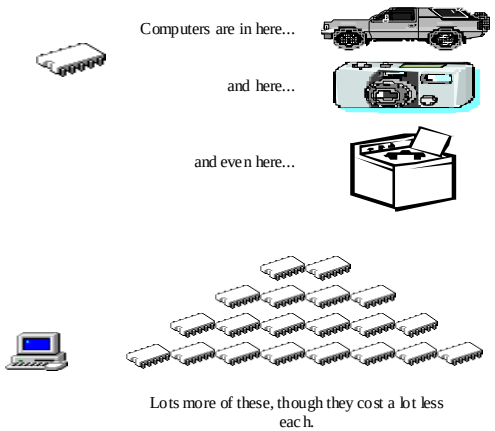
## Embedded systems overview

- Computing systems are everywhere
- Most of us think of “desktop” computers
  - PC’s
  - Laptops
  - Mainframes
  - Servers
- But there’s another type of computing system
  - Far more common...

Computing systems are everywhere, the most of us when think in embedded systems think in desktop computers, pc’s, laptops, mainframes, servers, but there are another type of computing system…

•

## Embedded systems overview

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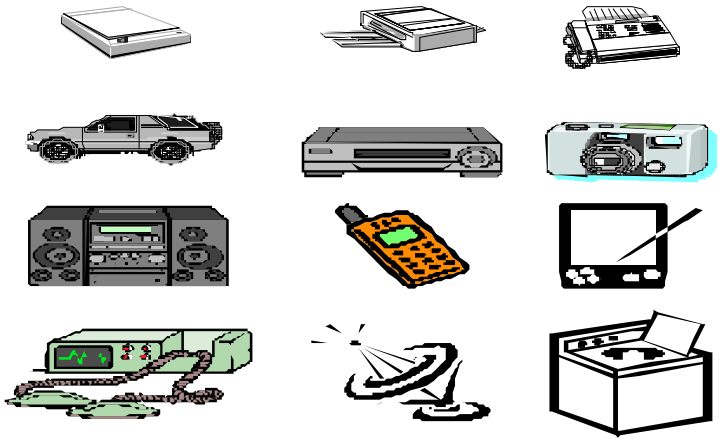
- Embedded computing systems
  - Computing systems embedded within electronic devices
  - Hard to define. Nearly any computing system other than a desktop computer
  - Billions of units produced yearly, versus millions of desktop units
  - Perhaps 50 per household and per automobile

# A “short list” of embedded systems



A list of embedded systems, but there are many mores!

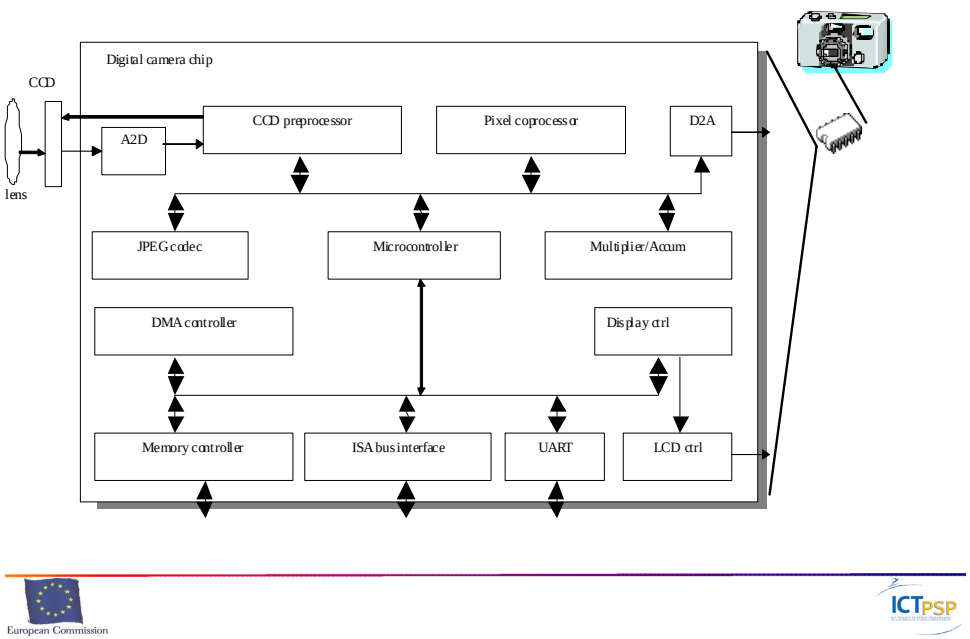
- Anti-lock brakes
- Auto-focus cameras
- Automatic teller machines
- Automatic toll systems
- Automatic transmission
- Avionic systems
- Battery chargers
- Camcorders
- Cell phones
- Cell-phone base stations
- Cordless phones
- Cruise control
- Curbside check-in systems
- Digital cameras
- Disk drives
- Electronic card readers
- Electronic instruments
- Electronic toys/games
- Factory control
- Fax machines
- Fingerprint identifiers
- Home security systems
- Life-support systems
- Medical testing systems
- Modems
- MPEG decoders
- Network cards
- Network switches/routers
- On-board navigation
- Pagers
- Photocopiers
- Point-of-sale systems
- Portable video games
- Printers
- Satellite phones
- Scanners
- Smart ovens/dishwashers
- Speech recognizers
- Stereo systems
- Teleconferencing systems
- Televisions
- Temperature controllers
- Theft tracking systems
- TV set-top boxes
- VCR’s, DVD players
- Video game consoles
- Video phones
- Washers and dryers

## Some common characteristics of embedded systems

- Single-functioned
  - –Executes a single program, repeatedly
- Tightly-constrained
  - –Low cost, low power, small, fast, etc.
- Reactive and real-time
  - –Continually reacts to changes in the system's environment
  - –Must compute certain results in real-time without delay

Common characteristics of embedded systems:

- Single e-functioned
- Tightly-constrained
- Reactive and real-time




An embedded system example -- a digital camera

- Single-functioned -- always a digital camera
- Tightly-constrained -- Low cost, low power, small, fast
- Reactive and real-time -- only to a small extent

## Design challenge – optimizing design metrics

•Obvious design goal:

–Construct an implementation with desired functionality

•Key design challenge:

–Simultaneously optimize numerous design metrics

•Design metric

– A measurable feature of a system’s implementation

–Optimizing design metrics is a key challenge

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Design challenge – optimizing design metrics

- Obvious design goal
- Key design challenge
- Design metric

## Design challenge – optimizing design metrics

- Common metrics
  - –Unit cost: the monetary cost of manufacturing each copy of the system, excluding NRE cost
  - –NRE cost (Non-Recurring Engineering cost): The one-time monetary cost of designing the system
  - –Size: the physical space required by the system
  - –Performance: the execution time or throughput of the system
  - –Power: the amount of power consumed by the system
  - –Flexibility: the ability to change the functionality of the system without incurring heavy NRE cost

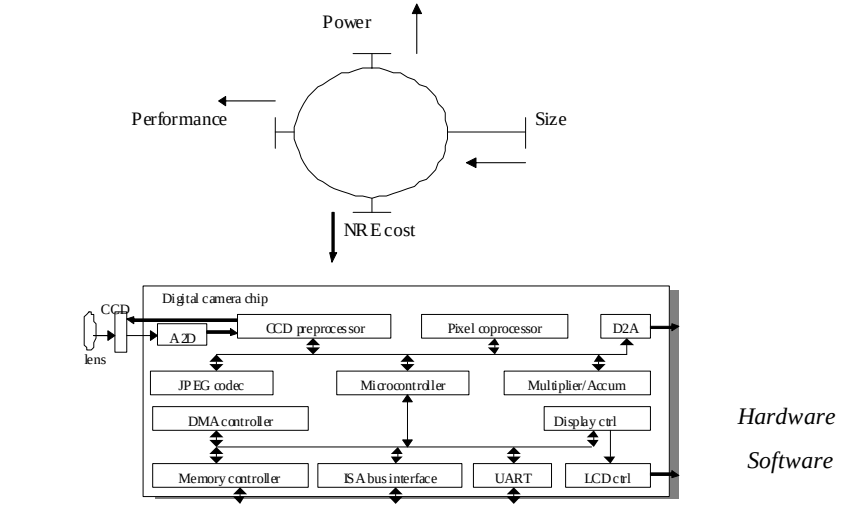
Design challenge – optimization design metrics

Common metrics: Unit cost, NRD cost, Size, Performance, Power and Flexibility.

## Design challenge – optimizing design metrics

- Common metrics (continued)
  - –Time-to-prototype: the time needed to build a working version of the system
  - –Time-to-market: the time required to develop a system to the point that it can be released and sold to customers
  - –Maintainability: the ability to modify the system after its initial release
  - –Correctness, safety, many more

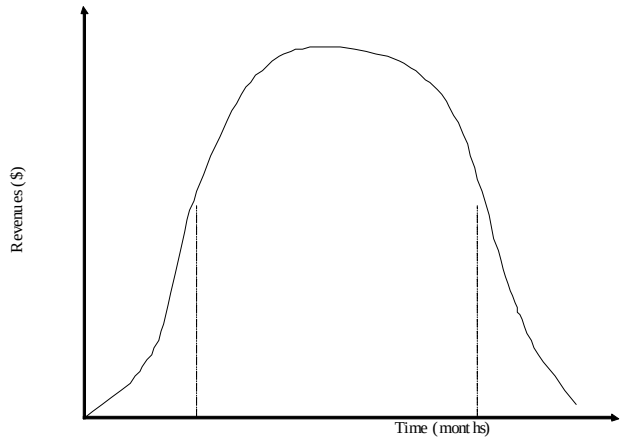
Common metrics (continued): Time-to-prototype, Time to market, Maintainability and Correctness.




Design metric competition -- improving one may worsen others

- Expertise with both **software and hardware** is needed to optimize design metrics
  - Not just a hardware or software expert, as is common
  - A designer must be comfortable with various technologies in order to choose the best for a given application and constraints

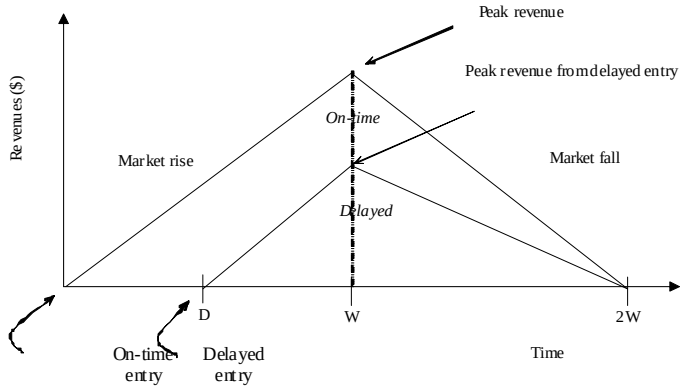
## Time-to-market: a demanding design metric




Time-to-market: a demanding design metric

- Time required to develop a product to the point it can be sold to customers
- Market window
  - Period during which the product would have highest sales
- Average time-to-market constraint is about 8 months
- Delays can be costly

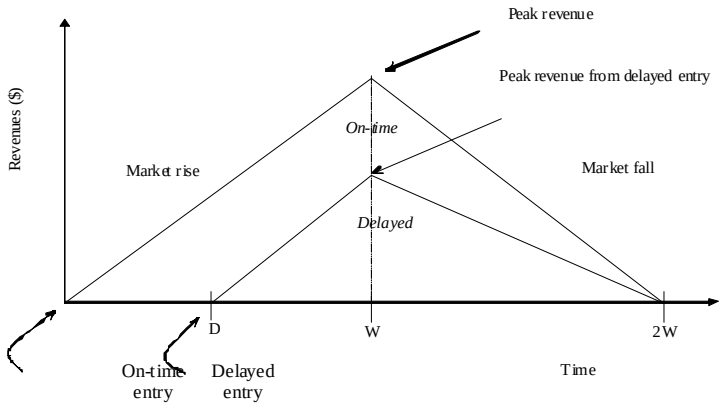
# Losses due to delayed market entry




Losses due to delayed market entry

- Simplified revenue model
  - Product life = 2W, peak at W
  - Time of market entry defines a triangle, representing market penetration
  - Triangle area equals revenue
- Loss
  - The difference between the on-time and delayed triangle areas

# Losses due to delayed market entry (cont.)




- Area = 1/2 * base * height
  - On-time = 1/2 * 2W * W
  - Delayed = 1/2 * (W-D+W)*(W-D)
- Percentage revenue loss = (D(3W-D)/2W2)*100%
- Try some examples
  - Lifetime 2W=52 wks, delay D=4 wks
  - (4*(3*26 –4)/2*26^2) = 22%
  - Lifetime 2W=52 wks, delay D=10 wks
  - (10*(3*26 –10)/2*26^2) = 50%
  - Delays are costly!

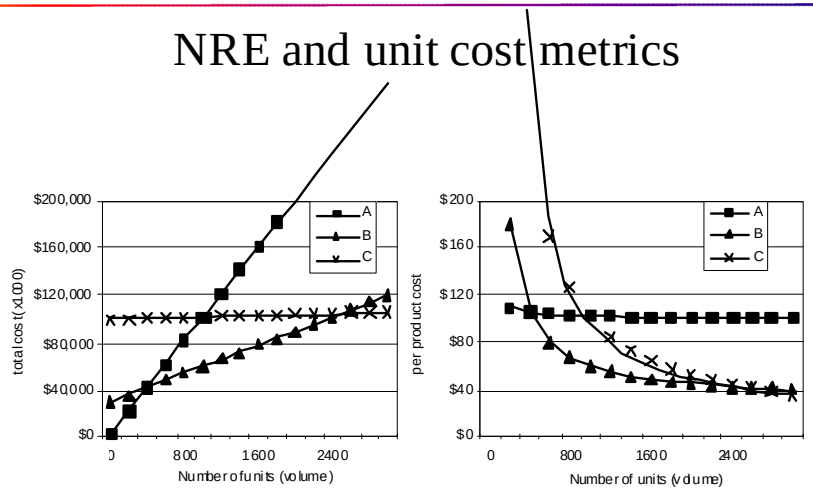
## NRE and unit cost metrics

•Example
  –NRE=$2000, unit=$100
  –For 10 units
    –total cost = $2000 + 10*$100 = $3000
    –per-product cost = $2000/10 + $100 = $300

NRE and unit cost metrics:

- Costs:
  - Unit cost: the monetary cost of manufacturing each copy of the system, excluding NRE cost
  - NRE cost (Non-Recurring Engineering cost): The one-time monetary cost of designing the system
  - *total cost = NRE cost + unit cost * # of units*
  - *per-product cost = total cost / # of units*
    *= (NRE cost / # of units) + unit cost*

## NRE and unit cost metrics




- Compare technologies by costs -- best depends on quantity
  - Technology A: NRE=$2,000, unit=$100
  - Technology B: NRE=$30,000, unit=$30
  - Technology C: NRE=$100,000, unit=$2

But, must also consider time-to-market

## The performance design metric

- Widely-used measure of system, widely-abused
  - Clock frequency, instructions per second – not good measures
  - Digital camera example – a user cares about how fast it processes images, not clock speed or instructions per second
- Latency (response time)
  - Time between task start and end
  - e.g., Camera's A and B process images in 0.25 seconds
- Throughput
  - Tasks per second, e.g. Camera A processes 4 images per second
  - Throughput can be more than latency seems to imply due to concurrency, e.g. Camera B may process 8 images per second (by capturing a new image while previous image is being stored).
- *Speedup* of B over S = B's performance / A's performance
  - Throughput speedup = 8/4 = 2

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The performance design metric:

Widely-used name of system, widely-abused (clock frequency, instruction per second – not good measures; digital camera example – a user cares about how it processes images, not clack speed or instruction speed).

Latency (time between star and end; e.g, Camera's A and B process image in o,25 seconds).

Throughput (tasks per second, e.g, Cameron A process 4 images per second; throughput can be more than latency seems to imply due to concurrency, e.g, Camera B may process 8 images per second).

Speedup of B over S = B's performance / A´s performance (throughput speedup = 8/4=2).

## Three key embedded system technologies

- Technology
  - –A manner of accomplishing a task, especially using technical processes, methods, or knowledge
- Three key technologies for embedded systems
  - –Processor technology
  - –IC technology
  - –Design technology

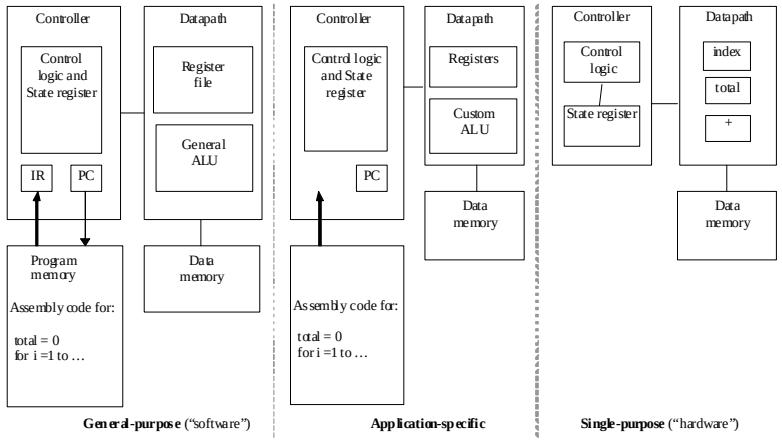
3 key embedded systems technologies:

Processor technology

IC technology

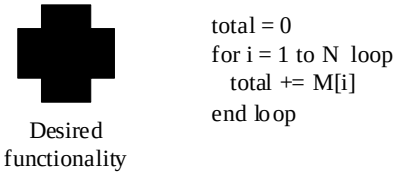
Design technology

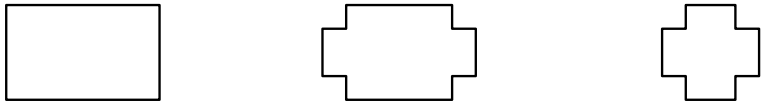
# Processor technology




- The architecture of the computation engine used to implement a system's desired functionality
- Processor does not have to be programmable
  - "Processor" *not* equal to general-purpose processor

# Processor technology



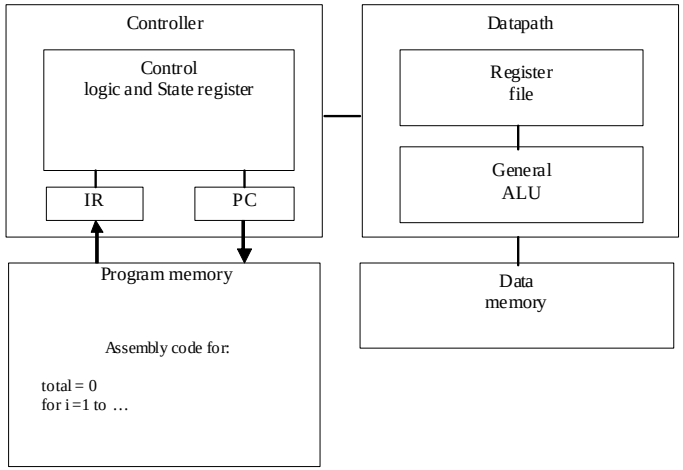
General-purpose processor

Application-specific processor

Single-purpose processor

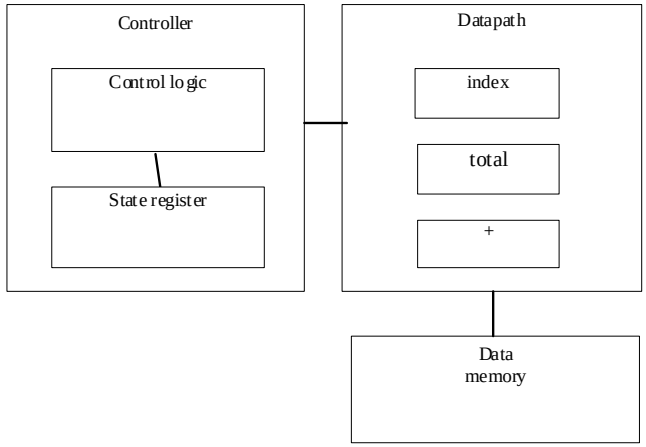
- Processors vary in their customization for the problem at hand.

# General-purpose processors



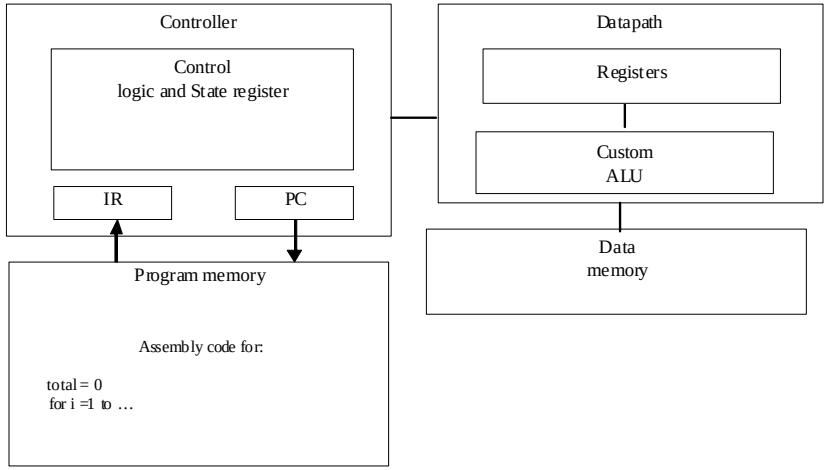

- Programmable device used in a variety of applications
  - Also known as “microprocessor”
- Features
  - Program memory
  - General datapath with large register file and general ALU
- User benefits
  - Low time-to-market and NRE costs
  - High flexibility
- “Pentium” the most well-known, but there are hundreds of others.

# Single-purpose processors



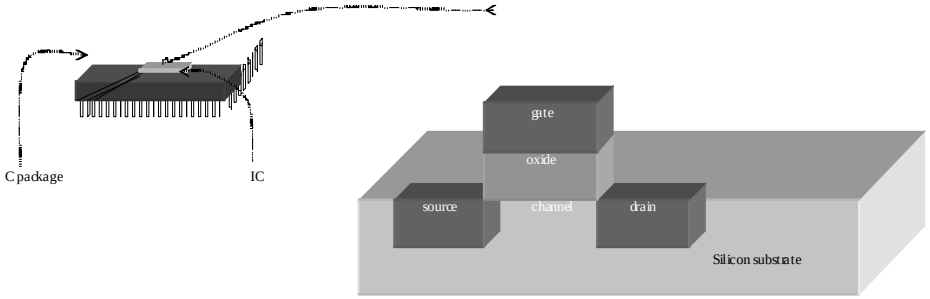

- Digital circuit designed to execute exactly one program
  - a.k.a. coprocessor, accelerator or peripheral
- Features
  - Contains only the components needed to execute a single program
  - No program memory
- Benefits
  - Fast
  - Low power
  - Small size

## Application-specific processors




- Programmable processor optimized for a particular class of applications having common characteristics
  - Compromise between general-purpose and single-purpose processors
- Features
  - Program memory
  - Optimized datapath
  - Special functional units
- Benefits
  - Some flexibility, good performance, size and power.

# IC technology




- The manner in which a digital (gate-level) implementation is mapped onto an IC
  - IC: Integrated circuit, or “chip”
  - IC technologies differ in their customization to a design
  - IC’s consist of numerous layers (perhaps 10 or more)
    - IC technologies differ with respect to who builds each layer and when

# IC technology

- Three types of IC technologies
  - –Full-custom/VLSI
  - –Semi-custom ASIC (gate array and standard cell)
  - –PLD (Programmable Logic Device)

3 types of IC technologies:

- Full – custom/ VLSI
- Semi – custom ASIC
- PLD

# Full-custom/VLSI

- All layers are optimized for an embedded system's particular digital implementation
  - Placing transistors
  - Sizing transistors
  - Routing wires
- Benefits
  - Excellent performance, small size, low power
- Drawbacks
  - High NRE cost (e.g., $300k), long time-to-market

Full – custom/VLSI

- all layers are optimized for an embedded system's particular digital implementation;
- Benefits excellent performance, small size, low power);
- Drawbacks (high NRE cost, long time-to-market.

# Semi-custom

- Lower layers are fully or partially built
  - –Designers are left with routing of wires and maybe placing some blocks
- Benefits
  - –Good performance, good size, less NRE cost than a full-custom implementation (perhaps $10k to $100k)
- Drawbacks
  - –Still require weeks to months to develop

Semi – custom

-lower layers are fully pr partial built;

- Benefices (good performance, good size, less NRE cost than a full – custom implementation);

- Drawbacks (still require weeks to months to develop).

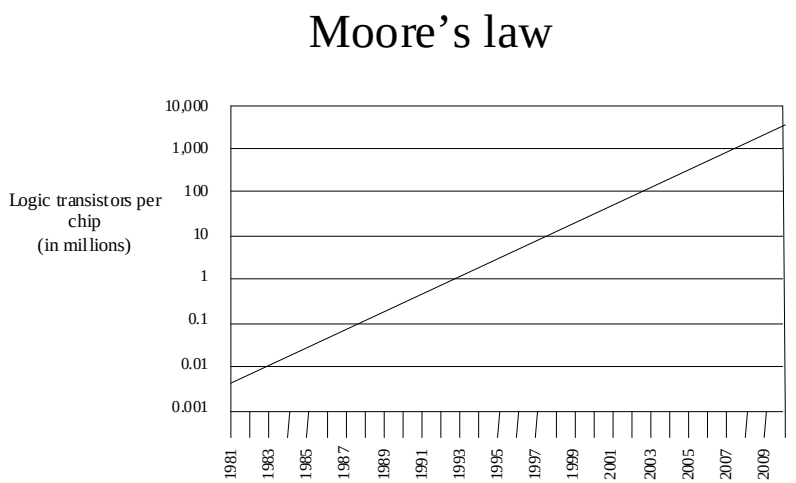
# PLD (Programmable Logic Device)

- All layers already exist
  - Designers can purchase an IC
  - Connections on the IC are either created or destroyed to implement desired functionality
  - Field-Programmable Gate Array (FPGA) very popular
- Benefits
  - Low NRE costs, almost instant IC availability
- Drawbacks
  - Bigger, expensive (perhaps $30 per unit), power hungry, slower

PLD (programmable logic device)

- All layers already exist (designers can purchase a IC, connections on the IC are either created or destroyed to implement desired functionality, field-programmable Gate Array (FPGA) very popular);
- Benefits (low NRE costs, almost instant IC availability);
- Drawbacks (bigger, expensive, power hungry, slower).

Moore’s law:




- The most important trend in embedded systems
  - Predicted in 1965 by Intel co-founder Gordon Moore

***IC transistor capacity has doubled roughly every 18 months for the past several decades***

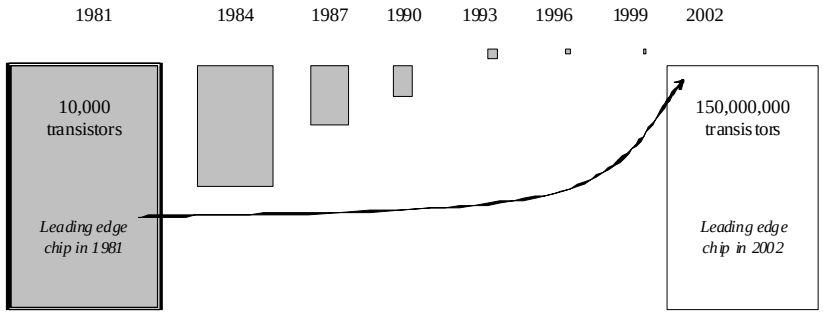
# Moore's law

- Wow
  - –This growth rate is hard to imagine, most people underestimate
  - –How many ancestors do you have from 20 generations ago
    - i.e., roughly how many people alive in the 1500's did it take to make you?
    - $2^{20}$ = more than *1 million people*
  - –*(This underestimation is the key to pyramid schemes!)*

Moore's law

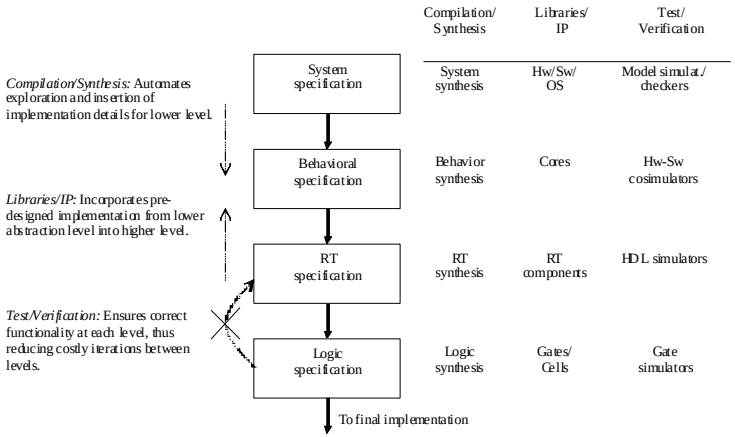
- This grow rate is hard to imagine, most people underestimate.
- How many ancestors do you have from 20 generations ago…

# Graphical illustration of Moore's law




- Something that doubles frequently grows more quickly than most people realize!
  - A 2002 chip can hold about 15,000 1981 chips inside itself.

# Design Technology




- The manner in which we convert our concept of desired system functionality into an implementation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**PARTNER NAME: INOVA+**

**CONTACT PERSON: MIGUEL SOUSA**

**GOOD PRACTICE NAME: NOE ON EMBEDDED SYSTEMS DESIGN**

**SOURCE OF THE GOOD PRACTICE: ARTISTITDESIGN NOE [HTTP://WWW.ARTIST-EMBEDDED.ORG]**

**TARGET GROUP: SMES**

**DATE: 30 NOVEMBER 2009**

ICT 2008

Lyon, November 25-27, 2008

# ArtistDesign

## NoE on Embedded Systems Design

Technical Coordinator: Bruno Bouyssounouse
VERIMAG Laboratory

http://www.artist-embedded.org/

ArtistDesign is a driving force for federating the European research community in Embedded Systems Design. It brings together 31 of the best research teams as core partners, 15 Industrial and SME affiliated Industrial partners, 25 affiliated Academic partners, and 5 affiliated International Collaboration partners who participate actively in the technical meetings and events.

## Concepts and Objectives – Main Ideas

**Main Idea 1**

*Embedded systems are essential to ensuring a leading position for Europe in key industrial sectors services. This is well-recognized in the ICT FP7 priorities, and through the ARTEMIS ETP.*

**Main Idea 2**

*Embedded systems design is an emerging scientific discipline, mobilizing a large international community, around a set of fundamental challenging and multi-disciplinary problems.*

*For this discipline to emerge, a considerable focused research effort by the best teams is needed.*

Concepts and Objectives – Main Ideas:

Embedded systems are essential to ensuring a leading position for Europe in key industrial sectors services.

Embedded systems design is an emerging scientific discipline, mobilizing a large international community, around a set of fundamental challenging and multi-disciplinary problems

## Theory, Methods and Tools for ES Design

*Design flow involves topics leading from initial requirements to a final implementation satisfying them. The objective is to study specific needs for these design activities, as well the possibility of integrating them in a coherent design flow.*

We distinguish four essential topics, for which existing techniques should be adapted and extended :

- **Modelling and Validation**: We need formal modelling techniques that take into account the characteristics of a system's external and execution environments. These techniques should support component-based construction for heterogeneous components to be applicable throughout the design process. For embedded systems, validation focuses on testing and verification of non functional properties, including performance and dependability.

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Theory, Methods and Tools for ES Design:

The objective of ArtistDesign is to study specific needs for design activities, as well the possibility of integrating them in a coherent design flow.

There are distinguishing four essential topics:

- Modelling and Validation: formal modelling techniques that take into account the characteristics of a system's external and execution environments. These techniques should support component-based construction for heterogeneous components to be applicable throughout the design process. For embedded systems, validation focuses on testing and verification of non functional properties, including performance and dependability.

## Theory, Methods and Tools for ES Design

**- Software Synthesis, Code Generation and Timing Analysis**: Strong integration should be sought for these interrelated topics. The aim is to study and implement resource-aware synthesis and code generation techniques. These techniques allow the generation of an implementation meeting given user requirements from a functional description of an application (e.g. application software) and a model of a target platform.

**- Real-Time Operating Systems Scheduling and Networks**: The aim is to develop theory methods and tools for new real-time software infrastructures, for the execution and communication between embedded applications. The main problems include adaptive resource management and dependability techniques, in particular to improve robustness to deviations from nominal conditions.

**- Platforms and MPSoC Design**: The aim is implementation of complex applications on multi-core HW platforms. It raises a number of problems for ensuring predictability and efficiency. These include adaptive techniques for resource management, and the study of reliable programming models for multi-core architectures.

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Theory, Methods and Tools for ES Design:

**- Software Synthesis, Code Generation and Timing Analysis**: Strong integration should be sought for these interrelated topics. The aim is to study and implement resource-aware synthesis and code generation techniques.

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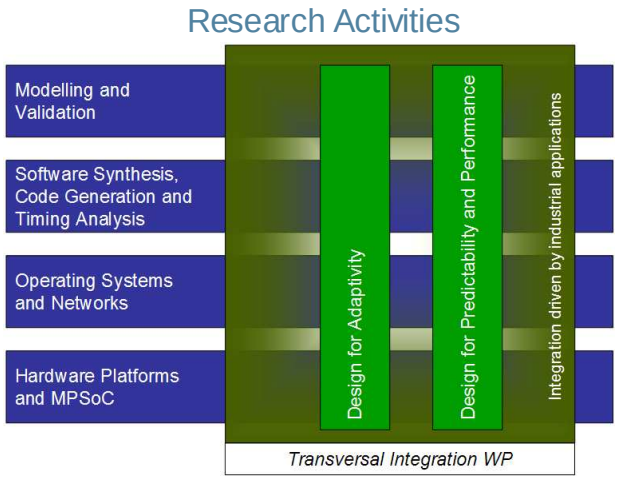


Research Activities:

Clusters are autonomous entities, with specific objectives, teams, leaders, and a dedicated yearly budget.

The set of Thematic Clusters cover all the main topics in Embedded Systems Design. The thematic activities in the Transversal Integration workpackage focus on Design methodologies, with specific objectives (Predictability, Adaptivity).

## Long Term Integration

Embedded systems design is a multidisciplinary area requiring competences from hardware engineering, operating systems and networks, programming and compilation, modelling and software engineering, control engineering. The ArtistDesign NoE gathers together leading European teams from all these areas. ArtistDesign will continue and extend these activities, both quantitatively and qualitatively. In setting up the consortium, we have sought the right balance between critical mass, excellence, and commitment from the core partners.

**- Critical Mass**

It was essential to gather a sufficient number of partners, to achieve a fair coverage of the main topics in the area, as well as to have the capacity to impact the European research landscape. Nonetheless, to ensure efficiency, we have limited the number of core partners, based on previous experience. At the same time, our impact is amplified through the large number of affiliated academic, SME, industrial, and international collaboration partners.

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Long Term Integration:

Embedded systems design is a multidisciplinary area requiring competences from hardware engineering, operating systems and networks, programming and compilation, modelling and software engineering, control engineering. The ArtistDesign NoE gathers together leading European teams from all these areas

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**-Critical Mass**: It was essential to gather a sufficient number of partners, to achieve a fair coverage of the main topics in the area, as well as to have the capacity to impact the European research landscape.

**- Excellence**

The ArtistDesign core partners include the main European leading teams, as attested by their leadership in their respective areas, as well as their strong involvement in national and European projects and initiatives.

**- Commitment**

The majority of the ArtistDesign core partners were already involved as core partners in the Artist2 NoE. They have demonstrated a high degree of investment to achieve the workprogramme objectives, by committing the resources needed, which are an order of magnitude larger than those provided by the NoE financing. We estimate that the effort for implementing the JPA is roughly 10 times the financial contribution for integration.

**- Excellence**: The ArtistDesign core partners include the main European leading teams, as attested by their leadership in their respective areas, as well as their strong involvement in national and European projects and initiatives.

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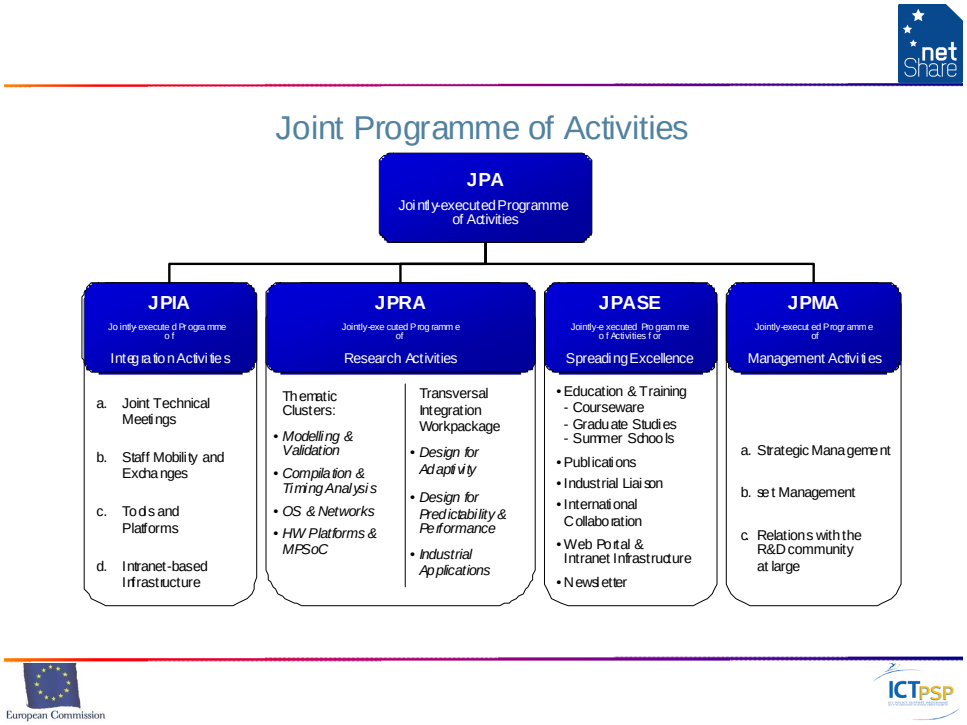
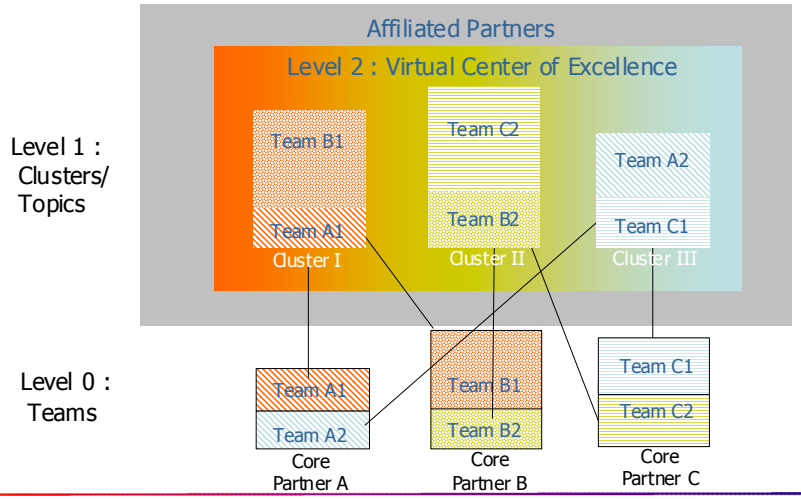



Joint Programme of Activities

ArtistDesign acts as a Virtual Centre of Excellence, composed of a set of virtual teams, called clusters. Each cluster gathers together selected teams from partners, to create the critical mass and expertise in one of the essential topics for embedded systems design.

## Principle of Construction



## Artist « Brand Recognition »

Artist has strong 'brand recognition' within the European and international community. This is visible through:

- **Role in ARTEMIS**. Partners involved: CEA, Bologna, ESI, IMEC, INRIA, Malardalen, OFFIS, PARADES, VERIMAG, TU Vienna,
  Areas: Automotive, avionics, real-time requirements for consumer electronics, multi-core processing, design methodologies
- **Organization of major conferences** (Embedded Systems Week, DATE, RTSS) as well as in IEEE and the ACM.
- **International Collaboration** activities (high-level meetings and schools)
- **Triggering important R&D projects** (national and European)
- **Individual roles**. Many teams play a leading role in their own countries, by participating in setting up and leading national centers of excellence and major projects.

The European embedded systems community is now a reality, through a structured constituency, as attested by strong presence in conferences, and significant interaction at all levels.

European Commission

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## Activities for Spreading Excellence

These NoE-level activities serve as a relay between the NoE and the international embedded systems design community at large.

**Education and Training** These serve as incubators for developing integrated curricula and materials, and to disseminate results and spread excellence well beyond the partners and affiliated partners of ArtistDesign.

**Publications in Conferences and Journals** Implemented through publication in the main conferences on Embedded Systems Design of the area, as well as the active participation for the organization and management of these events.

**Industrial Liaison** This consists of actions oriented towards affiliated industrial partners, to transfer results follow and get feedback on the research and integration activities in the JPA (JPRA, JPIA).

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**International Collaboration** These activities play a dual role: showcase the participants' results, and reinforce the NoE's leadership role worldwide. They also collect relevant information about evolution of the state of the art outside Europe.

**Web Portal** This will play a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large. The web portal is an essential mechanism for achieving integration and recognition.

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## Spreading Excellence – Schools Organized

Overall objective is the emergence of Embedded Systems Design as a scientific discipline. This objective is pursued within the international scientific and industrial community.

Three major schools per year:

- **ARTIST2 Summer School 2008 in Europe** *(5th edition)*
  *September 8-12, 2008 Autrans (near Grenoble), France*
- **Artist2 Summer School in China 2008** *(3rd edition)*
  *July 12-18, 2008 Shanghai, China*
- **ARTIST2 South-American School for Embedded Systems 2008** *(2nd edition)*
  *August 25-29, 2008 Universidade Federal de Santa Catarina, Florianopolis, Brazil*

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Additional schools organized by the NoE:

- **Real-Time Kernels for Microcontrollers: Theory and Practice**
  June 23-25, 2008 Pisa, Italy
- **ARTIST2 Graduate Course on: Automated Formal Methods for Embedded Systems 2008**
  *June 16-24, 2008 DTU - Lyngby, Denmark*
- **ARTIST2 Graduate Course on Embedded Control Systems**
  *May 26-30, 2008 Stockholm, Sweden*

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## Spreading Excellence – Workshops directly organized

Overall objective is the emergence of Embedded Systems Design as a scientific discipline. This objective is pursued within the international scientific and industrial community.

- **MoCC 2008**
  *July 3-4, 2008 Eindhoven, Netherlands*
- **WCET'08**
  *July 1st, 2008 Prague, Czech Republic*
- **OSPERT 2008**
  *July 1st, 2008 Prague, Czech Republic*
- **Movep'08**
  *June 23-27, 2008 Orleans, France*
- **COMES 2008**
  *June 17-18, 2008 Sigtuna, Sweden*
- **Mapping of Applications to MPSoCs**
  *June 16-17, 2008 Schloss Rheinfels, DE*
- **DataFlow Modeling for Embedded Systems**
  *May 5th, 2008 Pisa, Italy*
- **APRES'08**
  *April 21st, 2008 St. Louis, MO, USA*
- **SLA++P'2008**
  *April 5th, 2008 Budapest, Hungary*
- **ARTIST2 Timing Analysis activity meeting**
  *March 13th, 2008 Munich, Germany*
- **ATESST Open Workshop**
  *March 3rd, 2008 Brussels, Belgium*
- **Synchron 2007**
  *November 26-30, 2007 Bamberg, Germany*
- **ARTIST2 meeting on Integrated Modular Avionics**
  *November 12-13, 2007 Roma, Italy*
- **WESE'07: WS on Embedded Systems Education**
  *October 4-5, 2007 Salzburg, Austria*
- **Foundations of Component-based Design**
  *September 30th, 2007 Salzburg, Austria*
- **Between Control and Software**
  (in honor of Paul Caspi)
  *September 28th, 2007 VERIMAG - Grenoble, France*

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Spreading Excellence – Workshops directly organized:

Overall objective is the emergence of Embedded Systems Design as a scientific discipline. This objective is pursued within the international scientific and industrial community.

## Key Points for a Successful NoE

**Sizing / Scoping**
- Scope of the Technical Area Covered
- Size of the Consortium
- Excellence of the Partners
- Wholistic Viewpoint

**Internal Communication Mechanisms**
- Annual Plenary Meeting (at the Review)
- High-level events
- Mailing Lists
- Efficient Website (CMS)

**Evolvability of the NoE Structure**
- Budget is distributed according to activity
- Structural Flexibility (clusters, activities)
- Leadership Flexibility

**Dissemination**
- Website
- Events
- Strong Ties to Outside Teams
- Mailing Lists
- Scientific Publications
- Newsletters

**Reporting Mechanisms**
- Proactive Project Officer
- Choice of Reviewers
- Optimized Structure, Contents of the Deliverables
- Quality of the Reviews
- Streamlined Financial Reporting

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Key Points for a Successful NoE:

- Sizing / Scoping
- Internal Communication Mechanisms
- Evolvability of the NoE Structure
- Dissemination
- Reporting Mechanisms

Thanks and indication of the project site.

# THANK YOU

For further information:

http://www.artist-embedded.org/


**PROPOSAL/CONTRACT N.: 225004**

**PROJECT ACRONYM: NET-SHARE**

**PROJECT FULL TITLE: NETWORK OF ICT EXPERIENCED ORGANIZATIONS, SHARING EXPERIENCES, KNOWLEDGE AND SUPPORTING SME'S.**

**INSTRUMENT: ICT PSP**

**DURATION: 36 MONTHS**

**DISSEMINATION LEVEL: PUBLIC**

**PROJECT COORDINATOR ORGANISATION NAME:** Inovamais, S.A.; www.inovamais.pt

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**PARTNER NAME: INOVA+**

**CONTACT PERSON: MIGUEL SOUSA**

**GOOD PRACTICE NAME: MULTI – OBJECTIVE DESIGN SPACE EXPLORATION OF MULTI – PROCESSOR SOC ARCHITECTURE EMBEDDED MULTIMEDIA APPLICATIONS**

**SOURCE OF THE GOOD PRACTICE: MULTICUBE PROJECT [WWW.MULTICUBE.EU]**

**TARGET GROUP: SMES**

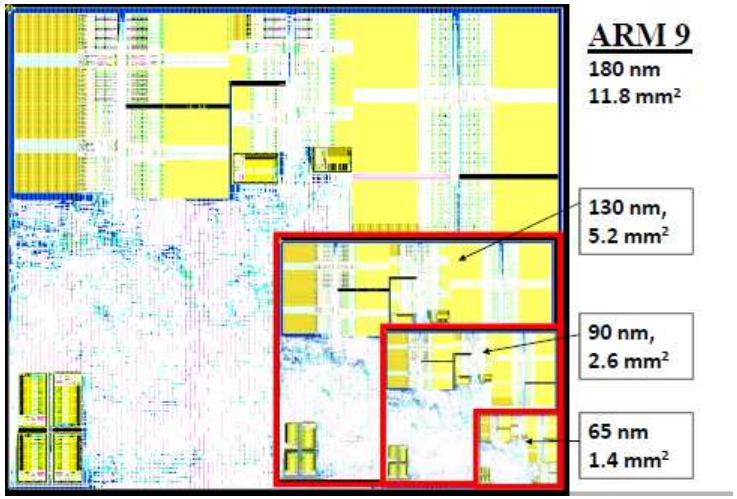
**DATE:**


**Multi – Objective Design Space Exploration Of Multi – Processor Soc Architecture Embedded Multimedia Applications**

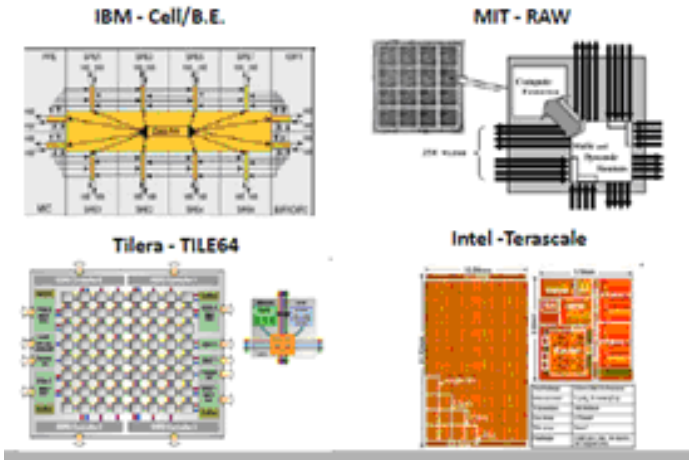
Many focused tools exist to optimize particular aspects of embedded systems. However, an overall design space exploration framework is needed to combine all the decisions into a global search space, and a common interface to the optimization and evaluation tools.

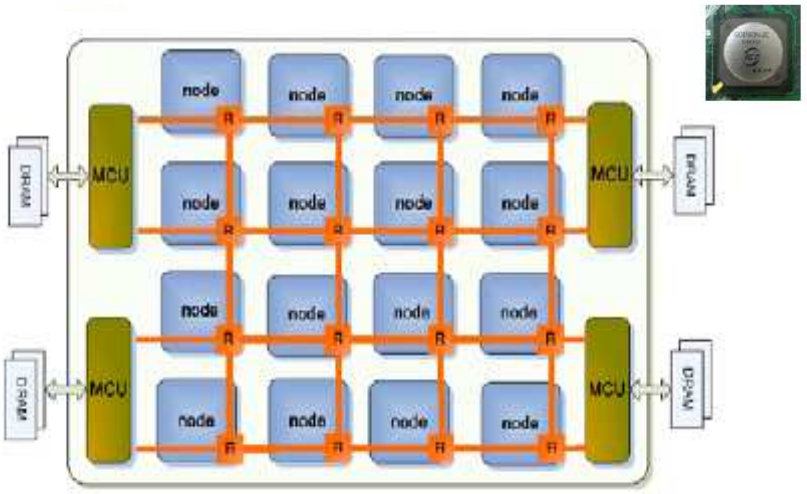
The MULTICUBE project focuses on the definition of an automatic multi-objective Design Space Exploration (DSE) framework to be used to tune the System-on-Chip architecture for the target application evaluating a set of metrics (e.g.
energy, latency, throughput, bandwidth, QoS, etc.) for the next generation embedded multimedia platforms.

Squeezing of computing cores



From multi-core to many-core architectures



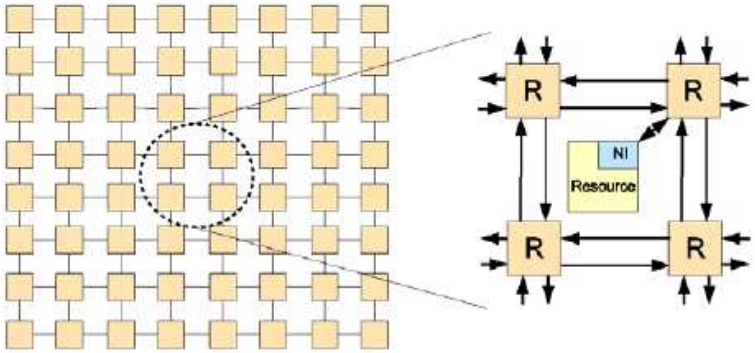



**Architecture of transformer**

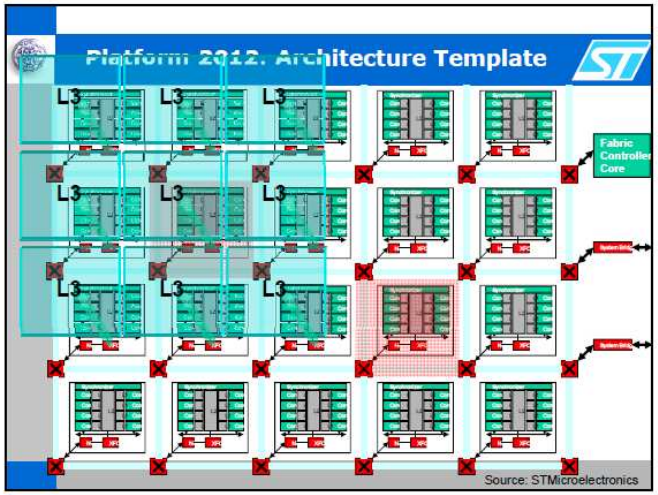
Transformer Processor Architecture consists of a 4*4 2D grid of identical compute elements, called nodes. Each node is a powerful computing system that can independently run an entire application

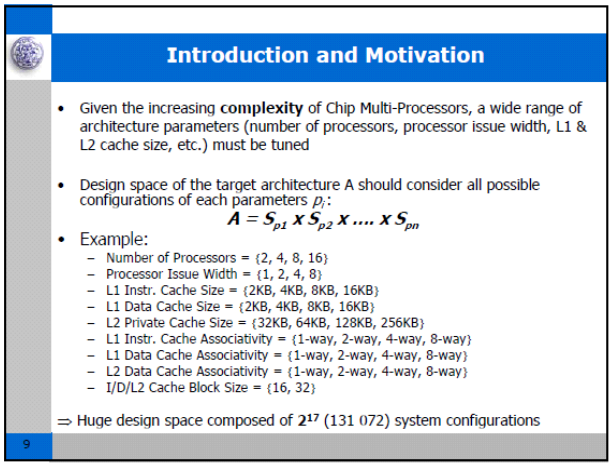
Multi – core architecture: a tied homogeneous multi – core architecture for general embedded purpose (Godson – T)

Many-core computing Fabric Template

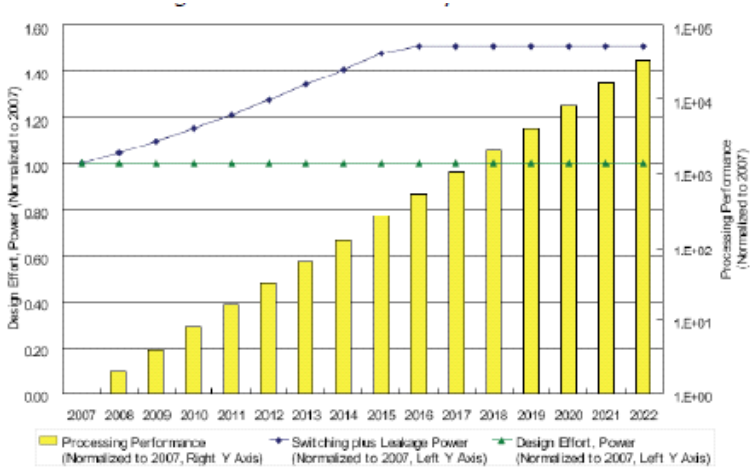


## Platform 2012. Architecture Template



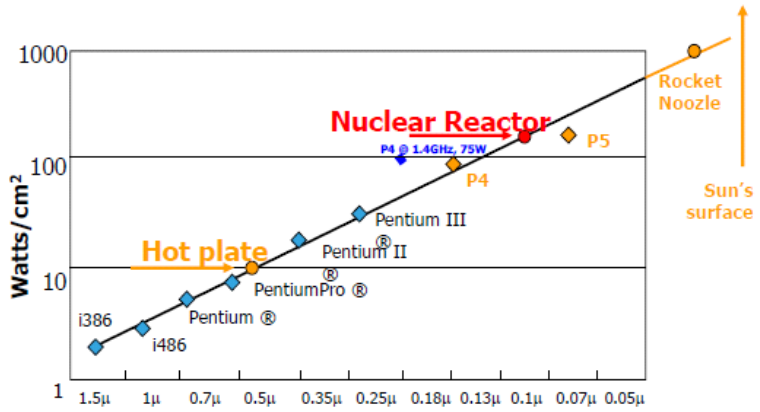


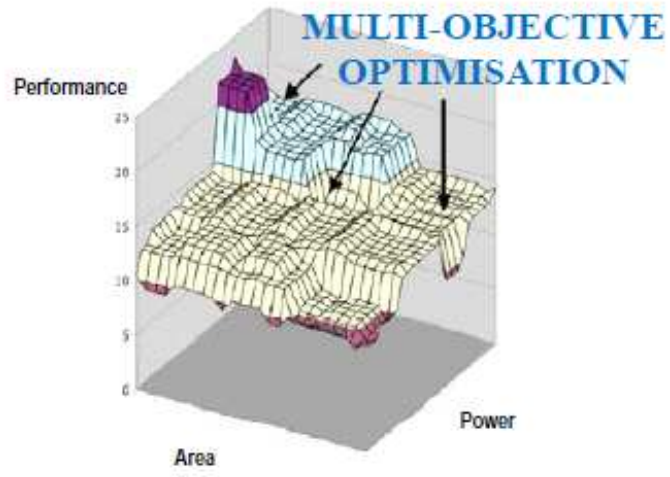

Given to the increase complexity of Chip Multi-processors, a wide range of architecture parameters must be tuned.



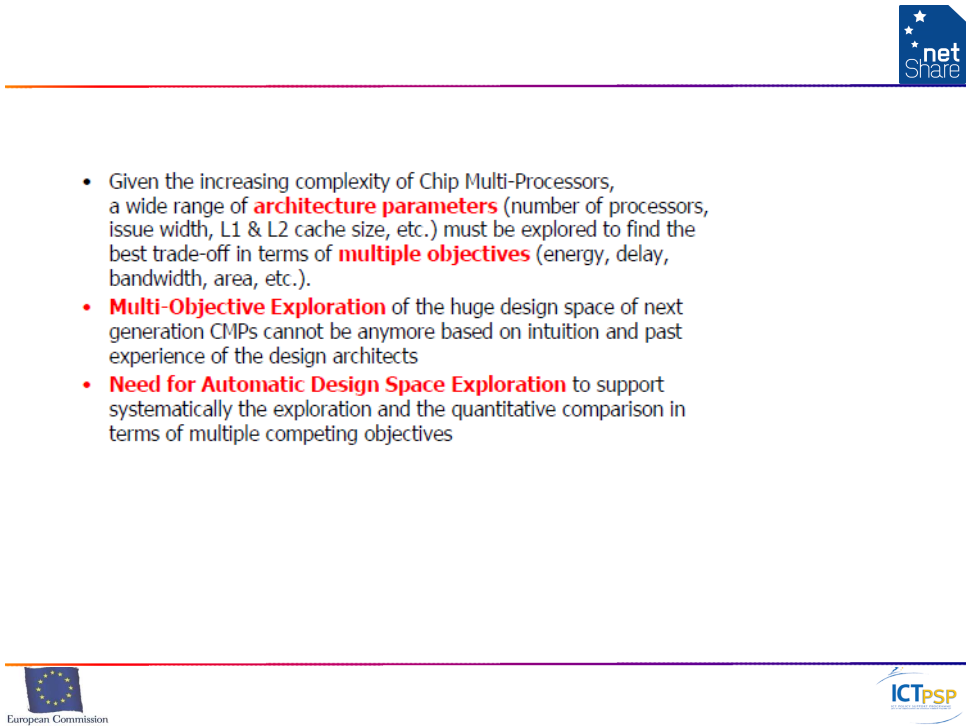

Processing performance is expected to grow more than 2 orders of magnitude in the next 10 years.

Power density trend for Intel´s microprocessors



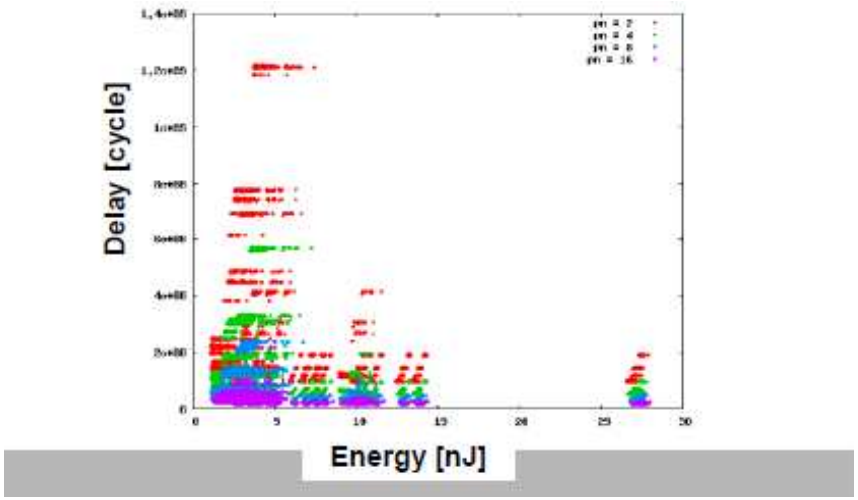



Soc requirements for MO plants (not only for performance processing)



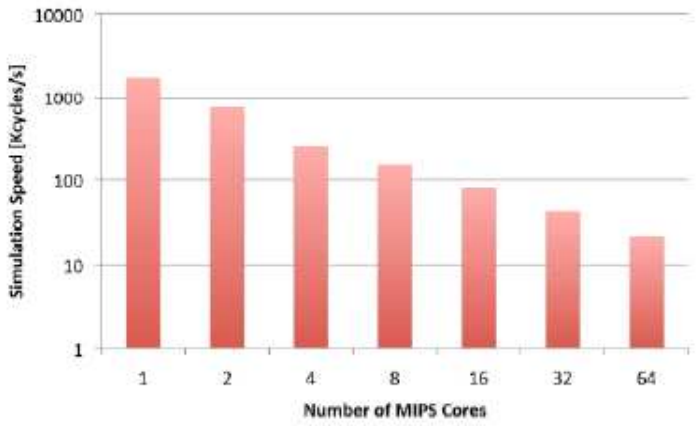

Introduction and Motivation

Given the increasing complexity of Chip-Processors, a wide range of architecture parameters must be explored to find the best trade-off in terms of multiple objectives. Exploration of the huge design space of next generation CMPs cannot be anymore based on intuition and past experience of the design architects. To support systematically the exploration ant the quantitative comparison in terms of multiple competing objectives there are need for automatic design space exploration.



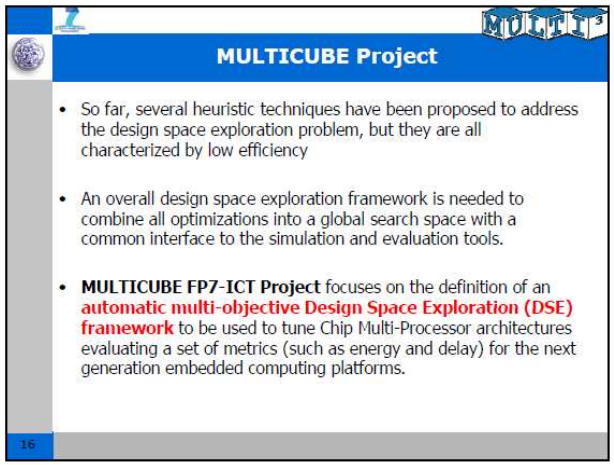

Full search design Space Exploration:

- in most cases , the design space to be explored is huge
- Automatic Design Space Exploration based on full-search exploration is unfeasible because its requires a very long simulation time
- Example: design space composed of 131 072 system configurations. If simulation of the target application for each system configuration requires 1min =131 072 min ~ 91 days for full search exploration.




SESC silumation speed by varying the number of MIPS cores

SESC is an open-source cycle accurate architectural simulator of MIPS instructions set, it models single processors and several configurations of CMPs, SECS project started at University of Illinois at Urbana – Champaign.




So far, several heuristic techniques have been proposed to address the design space exploration problem, but they are all characterized by low efficiency.

An overall design space exploration framework is need to combine all optimization into a global search space with a common interface to the simulation and evaluation tools.

MULTICUBE FP7-ICT Project focuses on the definition of an automatic multi-objective design space exploration framework to be a used tune Chip-Processor architectures evaluating set of metrics for the next generation embedded computing platforms.

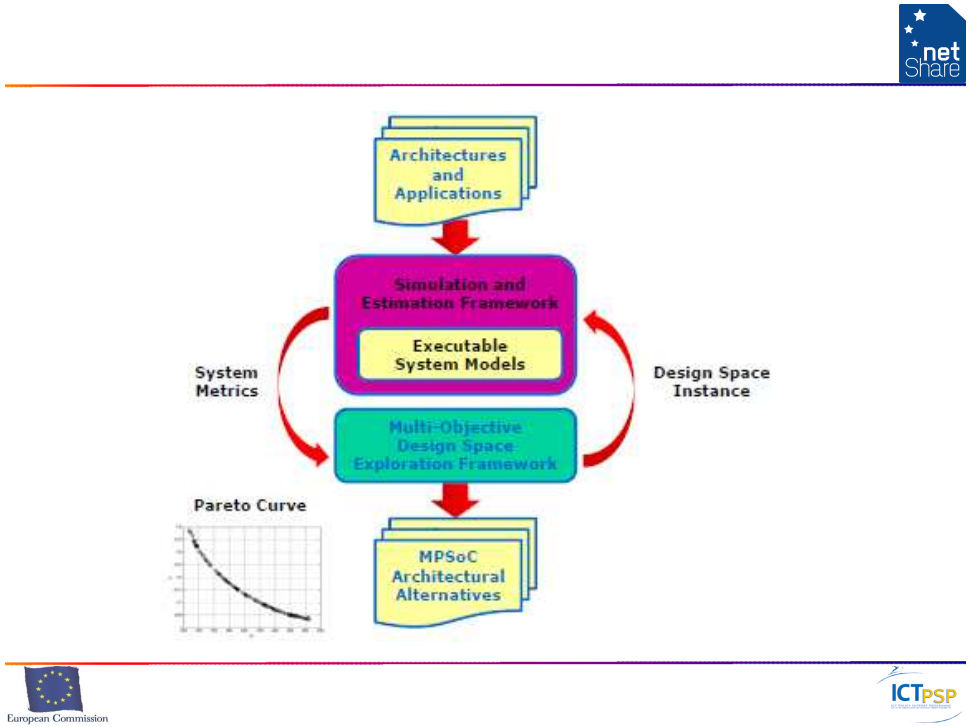
# Automatic Design Space Exploration


**MULTICUBE Project:**

*MULTI-Objective Design Space Exploration of Multi-Processor Soc Architecture for Embedded Multimedia Application*

Project duration: from January 2008 to June 2010

Patterns: Politecnico di Milano, DS2, STMicroelectronics, IMEC, ESTECO, Università della Svizzera Italiana, University of Cantabria, STMicroelectronics (China) and Institute of Computing Technology.

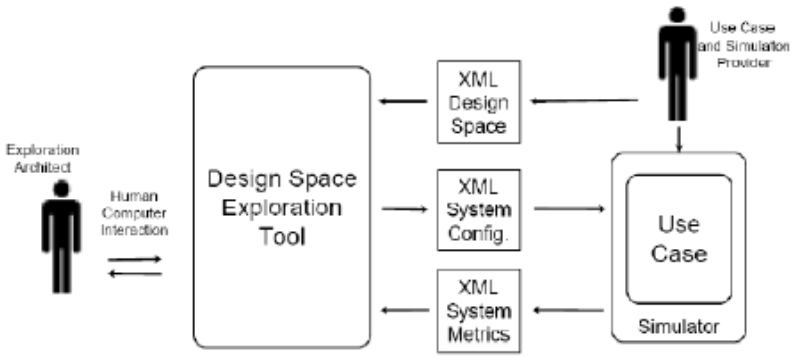



MULTICUBE Design flow

- The work proposes a **Multi-Objective Design Space Exploration (DSE) framework** to customize MP-SoC architectures evaluating a set of metrics.
- The DSE framework is simulation-based and focusing on:
  - **Design of Experiments**
  - **Response Surface Modeling**
- **Efficiency** of design space exploration in terms of minimizing the number of simulations
- **Flexible** DSE methodology: easy plug-in of system-level simulators and optimization techniques
- Framework implemented in a set of **open-source and proprietary tools**

MAIN GOALS:

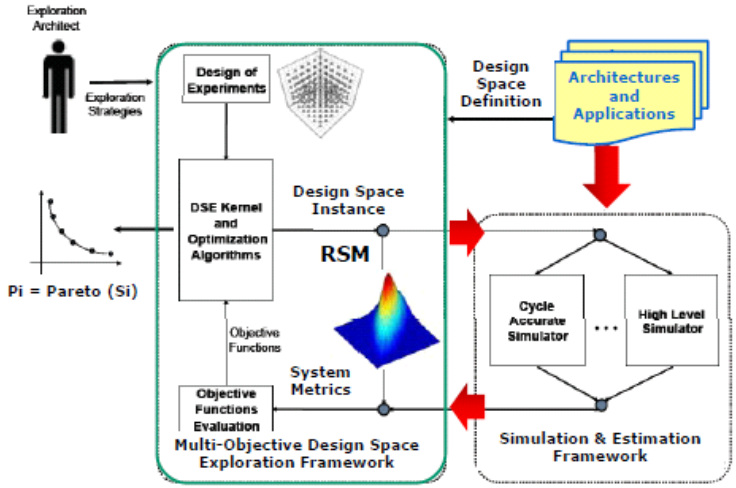
Multi-Objective Design Space Exploration (DSE) framework proposes to customize MP-SoC architectures evaluating a set of metric. The DSE is simulation-based and focusing on design of experiments and response surface modelling. DSE is efficient in terms of minimizing the number of simulations, is flexible because is easy plug-in of system-level simulation and optimization techniques.



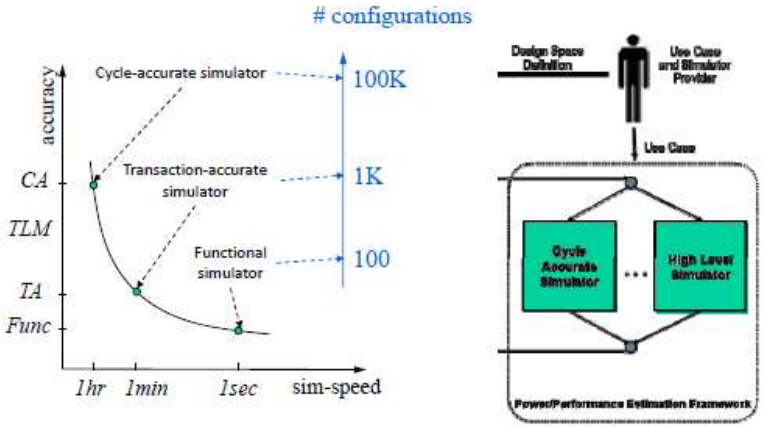

Design Flow Integration based on XML interface between design tools:

Definition of the specification for the design flow integration: The formal specification of the tool interface, based on the XML standard, if of fundamental importance for grating the seamless integration of design tools into a common design environment.

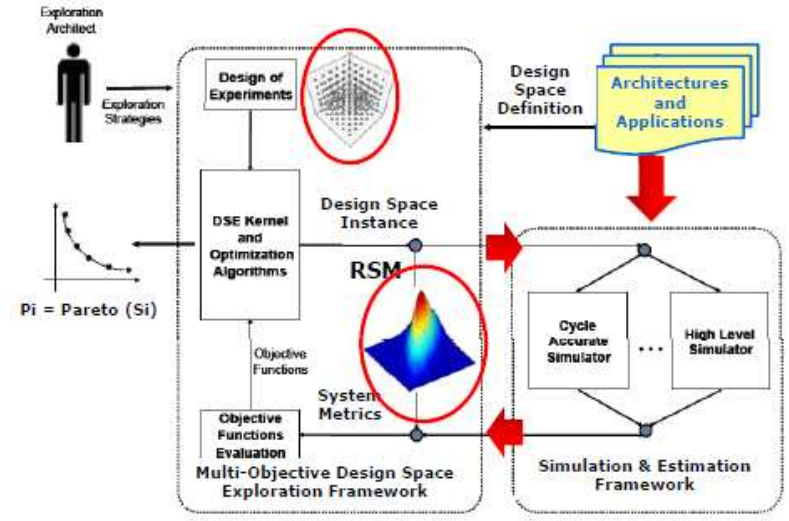
## Multi-Objective Design Space Exploration Flow



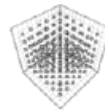
Multi-level simulations

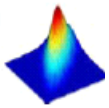


Multi-Objective Design Space Exploration Flow



- MO-DSE framework based on:
  - **Design of Experiments (DoEs):**
    To identify the experimentation plan where the set of tunable design parameters can vary
  - **Response Surface Modeling (RSM):**
    To use the set of data generated by DoE to obtain a response surface of the system behavior
- RSM based on two main phases:
  - During the **training phase,** known data (or training set) are used for tuning the RSM.
  - During the **prediction phase,** the RSM is used to predict the unknown system response.





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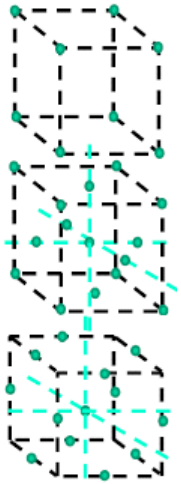
## Multi-Objective Design Space Exploration

MO-DSE framework based on a design of experiments (DoEs), to identify the experimentation plan where the set of tuneable design parameters can vary; and a response surface modelling (RSM), to use the set data generated by DoE to obtain a response surface of the system behaviour.

RSM based on 2 phases: during the training phase, know data are for tuning the RSM; during the prediction phase, the RSM is used to predict the unknown system response.

- Identifies the planning of experimentation campaign where the set of tunable design parameters can vary
- Specifies the **layout:** how to select the design points in the design space
- **Four DoE techniques have been applied:**
  - **Random**
  - **Full Factorial**
  - **Central Composite**
  - **Box Behnken**



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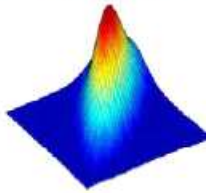
## Design of Experiments

Identifies the planning of experimentation campaign where the set of tuneable design parameters can vary; specifies the layout (how to select the design points in the design space);

4 DoE techniques have been applied: Random, Full factorial, Central composite and Box Behnken.

- RSM techniques are used to define an analytical dependence between design parameters and one or more response variables.
- To use the set of data generated by DoE to obtain a response model of the system behavior to forecast unknown system response.
- Four DoE techniques have been applied:
  - RSM based on Linear Regression
  - RSM based on Shepard's Interpolation
  - RSM based on Artificial Neural Networks
    - Three-layer fully-connected feed-forward ANNs
  - RSM based on Radial Basis Functions



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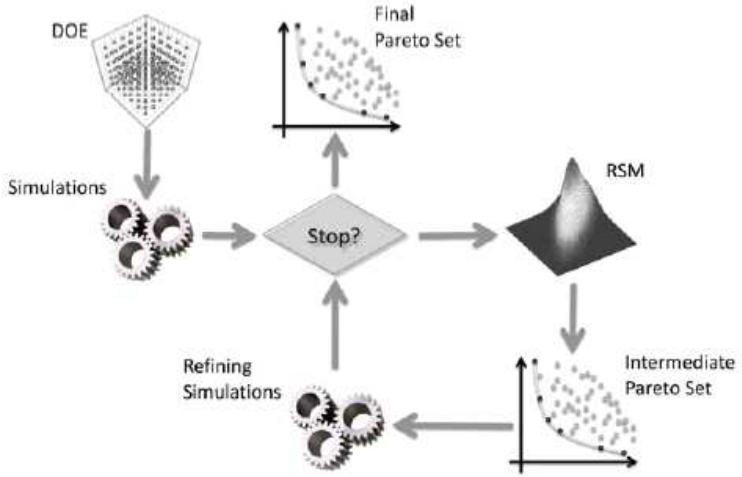
## Response Surface Modelling

RSM techniques are used to define an analytical dependence between design parameters and one more response variables. To use set data generated by DoE to obtain a response model of system behaviour to forecast unknown system response.

4 DoE techniques have been applied: RSM based on Linear Regression, RSM based on Shepard's Interpolation, RSM based on Artificial Neural Networks and RSM based on Radial Basis Function.

RSM –Support Interactive Pareto Refinement



## Target MP-SoC Architecture

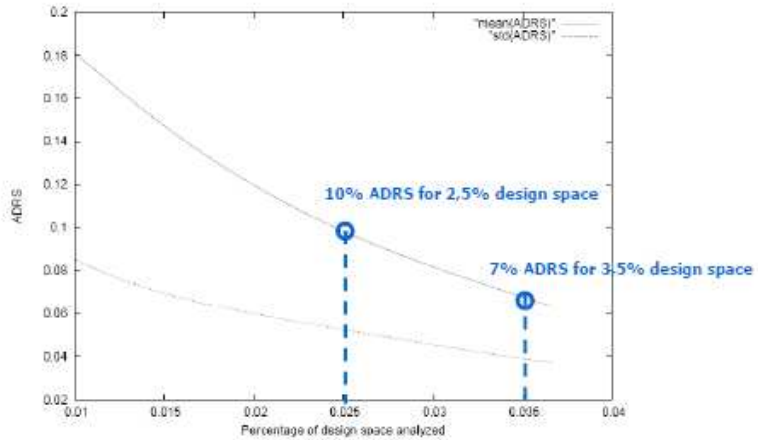
- MIPS-based shared memory MP-SoC with private caches
- Modeled with SESC simulator with power estimation support

| Parameter | Min. | Max. |
|---|---|---|
| # Processors | 2 | 16 |
| Processor issue width. | 1 | 8 |
| L1 instruction cache size | 2K | 16K |
| L1 data cache size | 2K | 16K |
| L2 private cache size | 32K | 256K |
| L1 instruction cache assoc. | 1w | 8w |
| L1 data cache assoc. | 1w | 8w |
| L2 private cache assoc. | 1w | 8w |
| I/D/L2 block size | 16 | 32 |

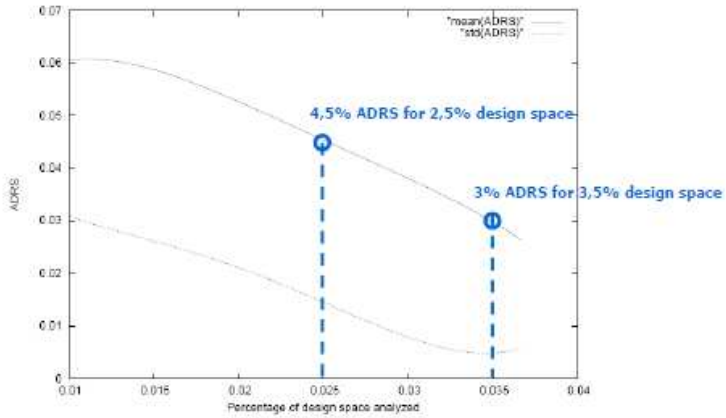
- Design space composed of $2^{17}$ design points (131 072)
- Four parallel applications {FFT, OCEAN, LU, RADIX} derived from SPLASH-2 benchmark suite for different data-sets

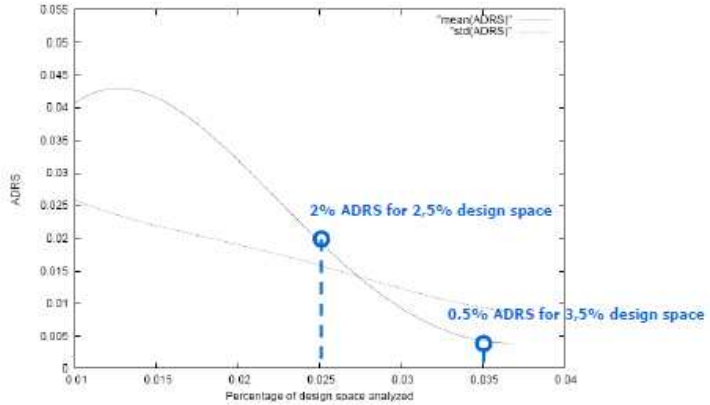
- Target multi-objective optimization problem:
  Minimization of ***average execution time*** and ***average [mW per MIPS]*** over the set of several application scenarios and subject to total cache size constraint
- Accuracy in terms of **Average Distance from Reference Set** to measure the distance between reference Pareto front and approximated Pareto front
  - **Lower ADRS, best approximated Pareto front**
- ADRS by varying the percentage of the design space analyzed from 1% to 3,5%
- Comparison with state-of-the-art heuristics:
  - **Multi-Objective Simulated Annealing (MOSA)**
  - **Non-dominated Sorting Genetic Algorithm (NSGA-II)**

Multi-Objective  Simulated Annealing (MOSA)



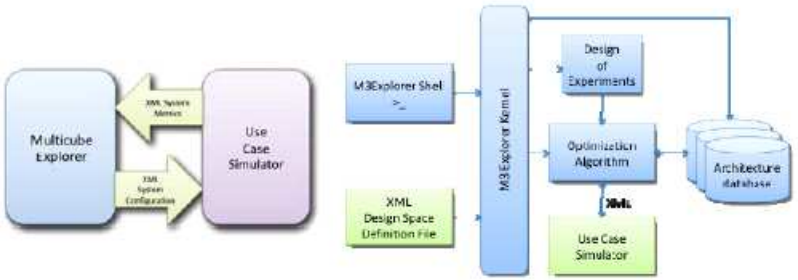
## Non-denominated Sorting Genetic Algorithm (NSGA II)




"mean(ADRS)"
"std(ADRS)"
ADRS
2% ADRS for 2,5% design space
0.5% ADRS for 3,5% design space
Percentage of design space analyzed


MULTICUBE Explorer

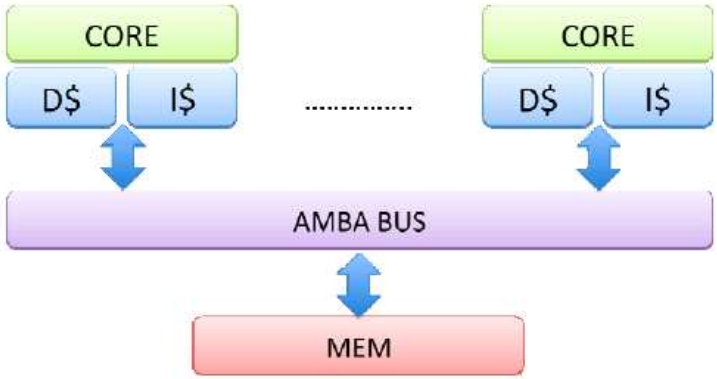
## MULTICUBE Explorer




Open-source prototype exploration framework (MULTICUBE Explorer): the tool enables a fast automatic optimization of parameterized system architectures towards a set of multiple objectives.

## Command Line Interface

Multi-processor Architecture: an example



Example of XML design space and metrics

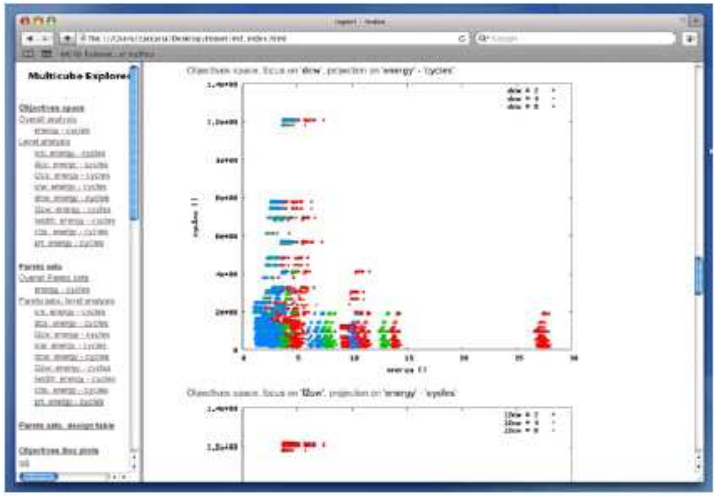
```
<?xml version="1.0" encoding ="UTF-8"?>
<design_space xmlns="http://www.multicube.eu/" version="1.3">
  <simulator>
    <simulator_executable
     path="/home/demo/tools/multicube-scope/qcif_example_v2/scope_example/script.sh" />
  </simulator>
  <parameters>
    rameter name="num_cpus" type="integer" min="2" max="8" />
    rameter name="icache_size" type="exp2" min="4096" max="32768"/>
    rameter name="freq" type="integer" min="40" max="200" step="40"/>
  </parameters>
  <rules>
    <rule>
      <not-equal>
        <parameter name="num_cpus"/> <constant value="3"/>
      </not-equal>
    </rule>
  </rules>
  <system_metrics>
    <system_metric name="latency" type="float" unit="Second" />
    ystem_metric name="instruction_count" type="float" unit="Instruction"/>
    ystem_metric name="power_consumption" type="float" unit="W" />
  </system_metrics>
</design_space>
```

Path

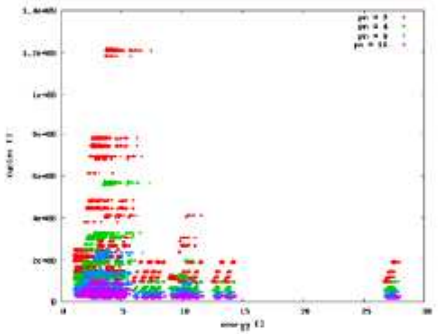
Parameters

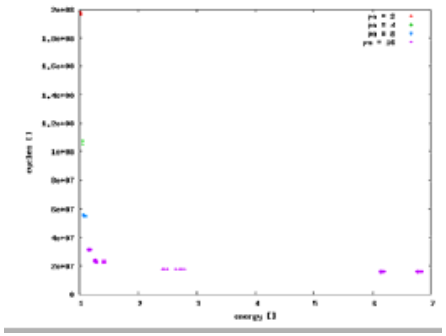
Rules

Metrics




Example of results (html format): Cycles and Energy objectives space





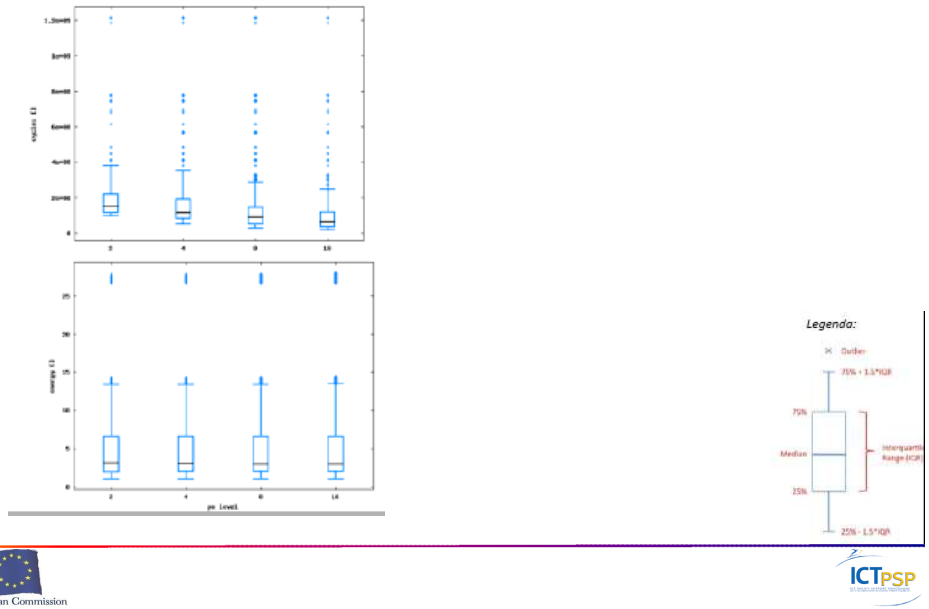
Cycles and Energy objectives space & Pareto curve

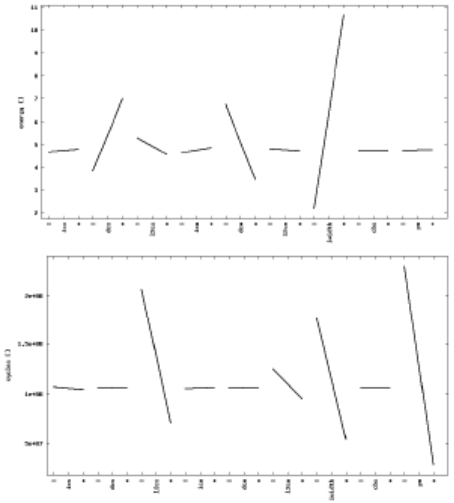
Table on the left: Cycles and energy objectives spaces associated with the design points with respect to parameter ‘pn’ number of processors.

Table on the right: Cycles and Energy Pareto curve associated with the design points with respect parameter ‘pn’ number of processors

## Box Plots

Showing the behaviour of each of the objectives (cycles, energy) associated to the design points with respect parameter ‘pn’ number of processors





Analysis of parameter main effects

Impact of the architecture parameters on each objective. The impact is computed as the average difference on the objectives by passing from a low (-) to a high (+) parameter setting.

- An automatic design space exploration methodology has been proposed leveraging Design of Experiments and Response Surface Modeling techniques
- The proposed methodology makes automatic exploration of CMP architectures more feasible
- The proposed approach can be easily combined with fast simulation techniques
- Future work: Joint architecture and compiler spaces to be explored
- This work is part of the ICT-FP7 EU project MULTICUBE

**www.multicube.eu**

Conclusions


**PROPOSAL/CONTRACT N.: 225004**

**PROJECT ACRONYM: NET-SHARE**

**PROJECT FULL TITLE: NETWORK OF ICT EXPERIENCED ORGANIZATIONS, SHARING EXPERIENCES, KNOWLEDGE AND SUPPORTING SME'S.**

**INSTRUMENT: ICT PSP**

**DURATION: 36 MONTHS**

**DISSEMINATION LEVEL: PUBLIC**

**PROJECT COORDINATOR ORGANISATION NAME:** Inovamais, S.A.; www.inovamais.pt

---

**PARTNER NAME: INOVA+**

**CONTACT PERSON: MIGUEL SOUSA**

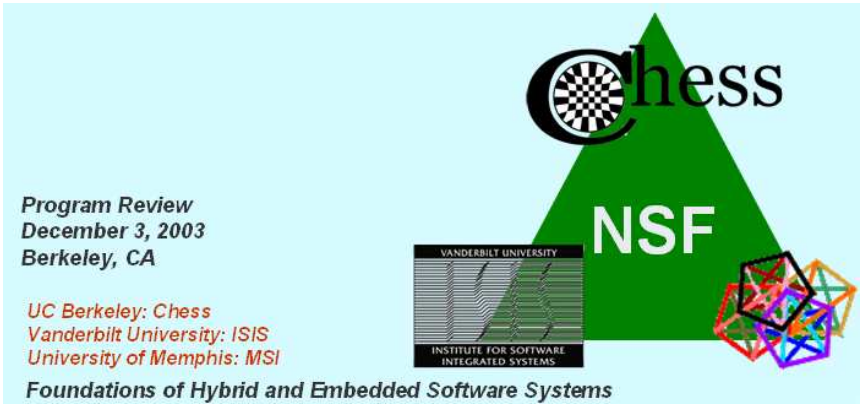
**GOOD PRACTICE NAME: FOUNDATIONS OF HYBRID AND EMBEDDED SOFTWARE AND SYSTEMS**

**SOURCE OF THE GOOD PRACTICE: NSF-ITR PROJECT**

**TARGET GROUP: SMES**

**DATE: 23 SEPTEMBER 2009**

**Foundations of Hybrid and Embedded Software and Systems: Overview of NSF-ITR Project**



# NSF-ITR Investigators

Ruzena Bajcsy, Ras Bodik, Bella Bollobas, Gautam Biswas,Tom Henzinger, Kenneth Frampton, Gabor Karsai, Kurt Keutzer, Edward Lee, George Necula, Alberto Sangiovanni Vincentelli, Shankar Sastry, Janos Sztipanovits, Pravin Varaiya.

Apresentation of NSF-ITR investigators

## ITR-Center Mission

- The goal of the ITR is to provide an environment for graduate research on the design issues necessary for supporting next-generation embedded software systems.
  - The research focus is on developing model-based and tool-supported design methodologies for real-time fault-tolerant software on heterogeneous distributed platforms.
- The Center maintains a close interaction between academic research and industrial experience.
  - A main objective is to facilitate the creation and transfer of modem, "new economy" software technology methods and tools to "old economy" market sectors in which embedded software plays an increasingly central role, such as aerospace, automotive, and consumer electronics.

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## Embedded Software: Problem for Whom?

- *DoD (from avionics to micro-robots)*
  - *Essential source of superiority*
  - *Largest, most complex systems*
- *Automotive (drive-by-wire)*
  - *Key competitive element in the future*
  - *Increasing interest but low risk taking*
- *Consumer Electronics (from mobile phones to TVs)*
  - *Problem is generally simpler*
  - *US industry is strongly challenged*
- *Plant Automation Systems*
  - *Conservative solutions to date*
  - *Emerging importance of SCADA/DCS in Critical Infrastructure Protection*

Embedded software systems is an problem for:

DoD

Automotive

Consumer Electronics

Plant Automotive Systems

## Key Properties of Hybrid & Embedded Software Systems

- Computational systems
  - but not first-and-foremost a computer
- Integral with physical processes
  - sensors, actuators
- Reactive
  - at the speed of the environment
- Heterogeneous
  - hardware/software, mixed architectures
- Networked
  - adaptive software, shared data, resource discovery
  - Ubiquitous and pervasive computing devices

Key proprieties:

Computational systems

Integral with physical process

Reactive

Heterogeneous

Networked

## Project Approach

- **Model-Based Design (the view from above)**
  - **principled frameworks for design**
  - **merging specification, modeling, and design**
  - **manipulable (mathematical) models**
  - **enabling analysis and verification**
  - **enabling effective synthesis of implementations**
- **Platform-Based Design (the view from below)**
  - **exposing key resource limitations**
  - **hiding inessential implementation details**
- **Tools**
  - **concrete realizations of design methods**

Tools – concrete realizations of design methods

The project approach is divided in 3 steps:

A model-based design

·principled frameworks for design

·merging specification, modeling, and design

·manipulable (mathematical) models

·enabling analysis and verification

·enabling effective synthesis of implementations

A platform-based design

·exposing key resource limitations

·hiding inessential implementation details

## Foundational Research

- **The science of computation has systematically abstracted away the physical world. The science of physical systems has systematically ignored computational limitations.** Embedded software systems, however, engage the physical world in a computational manner.
- **We believe that it is time to construct an Integrated Systems Science (ISS) that is simultaneously computational and physical.**
  Time, concurrency, robustness, continuums, and resource management must be remarried to computation.
- **Mathematical foundation: Hybrid Systems Theory: Modem Integrated Systems Science.**

The science of computation has systematically abstract away the physical world, and this has systematically ignored computational limitations. Embedded systems software systems engage the physical world in a computational manner. The project aims to construct Integrated Systems Science that is simultaneously computational and physical.

Mathematical foundation: Hybrid Systems Theory: modem integrated systems science.

## … and Embedded Software Research

- **Models and Tools:**
  - **Model-based design (platforms, interfaces, meta-models, virtual machines, abstract syntax and semantics, etc.)**
  - **Tool-supported design (simulation, verification, code generation, inter-operability, etc.)**
- **Applications:**
  - **Flight control systems**
  - **Automotive electronics**
  - **National experimental embedded software platform**
- **From resource-driven to requirements-driven embedded software development.**

Embedded Software Research based on:

Models and Tools:

Model-based design (platforms, interfaces, meta-models, virtual machines, abstract syntax and semantics, etc.)

Tool-supported design (simulation, verification, code generation, inter-operability, etc.)

Applications:

Flight control systems

Automotive electronics

National experimental embedded software platform

From resource-driven to requirements-driven embedded software development.

## Some Current Research Focus Areas

- Software architectures for actor-oriented design
- Interface theories for component-based design
- Virtual machines for embedded software
- Semantic models for time and concurrency
- Design transformation technology (code generation)
- Visual syntaxes for design
- Model checking hybrid systems
- Autonomous helicopters
- Automotive systems design

- Mobies
- SEC
- Fresco
- Ptolemy
- HyVisual
- Metropolis
- BEAR
- MESCAL

Areas of current research:

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Virtual machines for embedded software

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Automotive systems design

## “Center” Organization

- Funding Sources
  - Large NSF ITR
  - Other federal (NSF, DARPA, MURI, etc.)
  - Industrial (Participating Member Companies): IT and applications (automotive, aerospace, consumer electronics)
- Outreach
  - Curriculum development
  - Community colleges (EECS 20)
  - SUPERB program
  - SIPHER program

- National Experimental Platform for Hybrid and Embedded Systems and Software NEPHEST
- Embedded Software Consortium for Hybrid and Embedded Systems (ESCHER)

European Commission

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## NSF ITR Organization

- **PI:** Shankar Sastry
- **coPIs:** Tom Henzinger, Edward Lee, Alberto Sangiovanni-Vincentelli, Janos Sztipanovits
- **Participating Institutions:** UCB, Vanderbilt, Memphis State
- **Five Thrusts:**
  - Hybrid Systems Theory (Henzinger)
  - Model-Based Design (Sztipanovits)
  - Tool-Supported Architectures (Lee)
  - Applications: automotive (ASV), aerospace (Sastry)
  - Education and Outreach (Karsai, Lee, Varaiya)
- **Five year project: kick-off meeting November 14th , 2002. First Review May 8th, 2003, Second Review Dec 3rd, 2003.**
  - Weekly seminar series
  - Ptolemy workshop May 9th, 2003
  - NEST + CHESS Workshop May 9th, 2003

European Commission

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- Deep Compositionality
  - Assume Guarantee Reasoning for Hybrid Systems
  - Practical Hybrid System Modeling Language
  - Interface Theory for hybrid components
- Robust Hybrid Systems
  - Bundle Properties for hybrid systems
  - Topologies for hybrid systems
  - Stochastic hybrid systems
- Computational hybrid systems
  - Approximation techniques for H-J equations
  - Synthesis of safe and live controllers for hybrid systems
- Phase Transitions

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## Thrust II: Model Based Design

- Composition of Domain Specific Modeling Languages
  - Meta Modeling
  - Components to manipulate meta-models
  - Integration of meta-modeling with hybrid systems
- Model Synthesis Using Design Patterns
  - Pattern Based Modal Synthesis
  - Models of Computation
  - Design Constraints and Patterns for MMOC
- Model Transformation
  - Meta Generators
  - Scalable Models
  - Construction of Embeddable Generators

European Commission

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## Thrust III: Advanced Tool Architectures

- Syntax and Synthesis
  - Semantic Composition
  - Visual Concrete Syntaxes
  - Modal Models
- Interface Theories
- Virtual Machine Architectures
- Components for Embedded Systems

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## Thrust IV: Applications

- Embedded Control Systems
  - Avionics
  - Veitronics
  - Wireless Embedded Systems
- Embedded Systems for National/Homeland Security
  - Air Traffic Control
  - UAVs/UGVs
- Networks of Distributed Sensors
- Hybrid Models in Structural Engineering
  - Active Noise Control
  - Vibration damping of complex structures

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## Thrust V: Education and Outreach

- Curriculum Development for MSS
  - Lower Division
  - Upper Division
  - Graduate Courses
- Undergrad Course Insertion and Transfer
  - Goals and ABET requirement
  - New courses for partner institutions (workshop held March 1st 2003)
  - Introduction of new courses (will be replacing control course at upper division level by embedded software course)
  - New elective courses
  - Expansion of SUPERB program (6 + 4 students in Summer 03)
- Summer Internship Program in Embedded Software Research (SIPHER)

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## Outreach Continued

- Interaction with EU-IST programs
  - Columbus (with Cambridge, l'Aquila, Rome, Patras, INRIA)
  - Hybridge (with Cambridge, Patras, NLR, Eurocontrol, Brescia, KTH)
  - ARTISTE: Educational Initiatives (Grenoble, INRIA, ETH-Zurich)
- Foundation of non-profit ESCHER
  - Interaction with F-22/JSF designs
  - Secure Networked Embedded Systems

There are continued outreach troughs the interaction with EU-IST programs (Colombus, Hybridge, ARTIST) and the Foundation of non-profit ESCHER (interaction with F-22/JSF designs, Secure Network Systems)

## Management Plan

- Executive Board (Pis and co-Pis)
- Thrust Leaders
  - Hybrid Systems: Henzinger
  - Model Based Tool Design: Sztipanovits
  - Integrated Tool Architectures: Lee
  - Applications: Sangiovanni-Vincentelli
  - Education: Lee, Varaiya
  - Outreach: Karsai, Williams
- Industrial Advisory Board
  - First meeting May 7th 2003
  - Sustained interaction with GM, Boeing, Ford, Lockheed, Raytheon to found ESCHER.
  - Industrial partners: above + Honeywell, Toyota, Daimler Chrysler, Windriver

The management plan consists on an Executive Board, thrust leaders and an Industrial Advisory Board

## Emerging Research Area: Embedded Systems for Homeland Security

**Technology needs were classified into areas:**

- **Information Assurance and Survivability**
- **Security with Privacy**
- **Secure Network Embedded Systems (SENSE)**
- **Validated Hybrid Systems models for interdependencies of infrastructures**
- **Public Private Partnerships for Technology Transition**

New areas for embedded systems are emerging, namely for homeland security. The technologies needs were classified into areas as information assurance and survivability, security with privacy; secure network embedded systems; validated hybrid systems models for interdependencies of infrastructures and public private partnerships for technology transition.


Critical Infrastructures:

- Government operations
- Gas & oil storage and delivery
- Telecommunications
- Emergency services
- Electrical energy
- Water supply systems
- Banking & finance
- Transportations

## Secure SCADA and beyond

**We think that there is a great deal to be done in terms of operationalizing secure versions of SCADA (Supervisory Control And Data Acquisition) and DCS (Digital Control Systems) for the infrastructures considered, especially power, natural gas, chemical and process control, etc. However, the sense was that this infrastructure was going to be gradually replaced by networked embedded devices (possibly wireless) as computing and communication devices become more ubiquitous and prevalent. Thus, the major research recommendations were for an area that we named** Secure Networked Embedded Systems (SENSE).

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The sense was that this infrastructure was going to be gradually replaced by net worked embedded devices as computing and communication on devices become more ubiquities and prevalent. Thus, the major research recommendations were for an area called Secure Network Embedded Systems (SENSE).

## SCADA of the Future

- Current SCADA
  - Closed systems, limited coordination, unprotected cyber-infrastructure
  - Local, limited adaptation (parametric), manual control
  - Static, centralized structure
- Future requirements
  - Decentralized, secure open systems (peer-to-peer, mutable hierarchies of operation)
  - Direct support for coordinated control, authority restriction
  - Trusted, automated reconfiguration
    - Isolate drop-outs, limit cascading failure, manage regions under attack
    - Enable re-entry upon recovery to normal operation
    - Coordinate degraded, recovery modes
  - Diagnosis, mitigation of combined physical, cyber attack
  - Advanced SCADA for productivity, market stability, manageability

Scada, in the future, will needs a decentralized, secure systems (peer-to-peer, mutable hierarchies of operation); Direct support for coordinated control, authority restriction; Trusted, automated reconfiguration (Isolate drop-outs, limit cascading failure, manage regions under attack; Enable re-entry upon recovery to normal operation, Coordinate degraded, recovery modes); Diagnosis, mitigation of combined physical, cyber attack and Advanced SCADA for productivity, market stability, manageability.

## Secure Network Embedded Systems

**Embedded Software prevalent in all critical infrastructures. Critical to high confidence embedded software are open source techniques for**

- **Automated Design, Verification and Validation**
  - **Verified design in a formal, mathematical sense**
  - **Validated design in an engineering sense**
  - **Certifiable design to allow for regulatory and certification input**
- **High Confidence Systems**
  - **Narrow waisted middleware**
    - **Trusted abstractions, limited interfaces**
    - **Algorithms and protocols for secure, distributed coordination and control**
  - **Security and composable operating systems**
  - **Tamper Proof Software**
- **Generative Programming**
- **Intelligent Microsystems: infrastructure of the future with security codesign with hardware and software.**

Embedded Software prevalent in all critical infrastructures. Critical to high confidence embedded software are open source techniques for automotive design, high control confidence systems, generative programming and intelligent Microsystems.

## Layers of Secure Network Embedded Systems

- **Physical Layer**
  - Attacks: jamming, tampering
  - Defenses: spread spectrum, priority messages, lower duty cycle, region mapping, mode change, tamper proofing, hiding.
- **Link Layer**
  - Attacks: collision, exhaustion, unfairness
  - Defenses: error correcting code, rate limitation, small frames

Layers of Secure Network Embedded Systems:

Physical Layer (attacks: jamming, tampering; defences: spread spectrum, priority messages, lower duty cycle, region mapping, mode change, tamper proofing, hiding).

Link Layer (attacks: collision, exhaustion, unfairness; defences: error correcting code, rate limitation, small frames).

## Layers of Secure Network Embedded Systems

- Network and Routing Layer
  - Attacks: neglect and greed, homing, misdirection, black holes
  - Defenses: redundancy, probing, encryption, egress filtering, authorization, monitoring, authorization, monitoring, redundancy
- Transport Layer
  - Attacks: flooding, desynchronization
  - Defenses: client puzzles, authentication
- Embedded System/Application Layer
  - Attacks: insider misuse, unprotected operations, resource overload attacks, distributed service disruption
  - Defenses: authority management (operator authentication, role-based control authorization), secure resource management, secure application distribution services

Layers of Secure Network Embedded Systems:

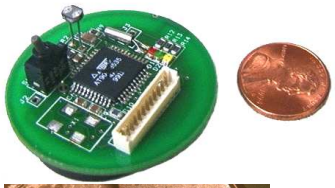
Network and Routing Layer (attacks: neglect and greed, homing, misdirection, black holes; defences: redundancy, probing, egress filtering, authorization, monitoring, authorization, redundancy).

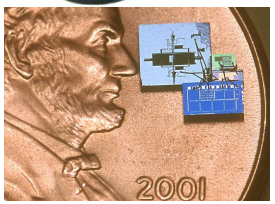
Transport Layer (attacks: flooding, desynchronization; defences: client puzzles, authentication).

Embedded System/application Layer (attacks: insider misuse, unprotect operation, resource overload attacks, distributed service disruption; defences: authority management, secure resource management, secure application distribution services).

## Foundations: Smart Dust and Motes

**Berkeley experimental platforms:**






Fundation: Smart Dust and Motes

Atmel ATMEGA103

- 4 Mhz 8-bit CPU
- 128KB Instruction Memory
- 4KB RAM

4 Mbit flash (AT45DB041B)

- SPI interface, 1-4 uj/bit r/w

RFM TR1000 radio

- 50 kb/s
- Sense and control of signal strength

Network programmable in place

Multihop routing, multicast

Sub-microsecond RF node-to-node synchronization

Provides unique serial ID's

Sensor board: acoustic and magnetic sensors

## Modeling: Research Needs

- New Modeling and Simulation Tools for Hybrid Systems. CIP systems involve multiple models of computation (discrete, continuous, logical, differential equations) and many hierarchical levels and granularities. Simulators for such systems need to be made numerically robust and probabilistically accurate.
- Tools for the assessment of level of risk. Risk assessment for determination of deployment of fixed budget to most critical areas.
- Development of simulation test-beds for red-teaming exercises, interdependency evaluation, response preparation and assessment.

Research needs: New modelling and simulation tools for hybrid systems (CIP systems involve multiple models of computation and hierarchical levels and granularities. Simulators for such systems need to be made numerically robust and probability accurate).

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**PROPOSAL/CONTRACT N.: 225004**

**PROJECT ACRONYM: NET-SHARE**

**PROJECT FULL TITLE: NETWORK OF ICT EXPERIENCED ORGANIZATIONS, SHARING EXPERIENCES, KNOWLEDGE AND SUPPORTING SME'S.**

**INSTRUMENT: ICT PSP**

**DURATION: 36 MONTHS**

**DISSEMINATION LEVEL: PUBLIC**

**PROJECT COORDINATOR ORGANISATION NAME:** Inovamais, S.A.; www.inovamais.pt

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**PARTNER NAME: WIT**

**CONTACT PERSON: SINEAD QUEALY**

**GOOD PRACTICE NAME: Network-centric Middleware for group communications and resource sharing across heterogeneous embedded systems**

**SOURCE OF THE GOOD PRACTICE: MORE**

**TARGET GROUP:** Embedded-electronics

**DATE: 04/06/09**

Grant Agreement: 225004

# NET-SHARE

***MORE***

**Network-centric Middleware for group communications and resource sharing across heterogeneous embedded systems**

- IST funded
- Start Date: June 1st 2006 - 36 months duration
- Under Directorate G Unit G3 – Embedded Systems
- Total Funds €2.7m
- 7 Partners

**End User scenarios**

1. Remote health monitoring, specifically for diabetics
2. Mitigation management of environmental damage in the forestry domain

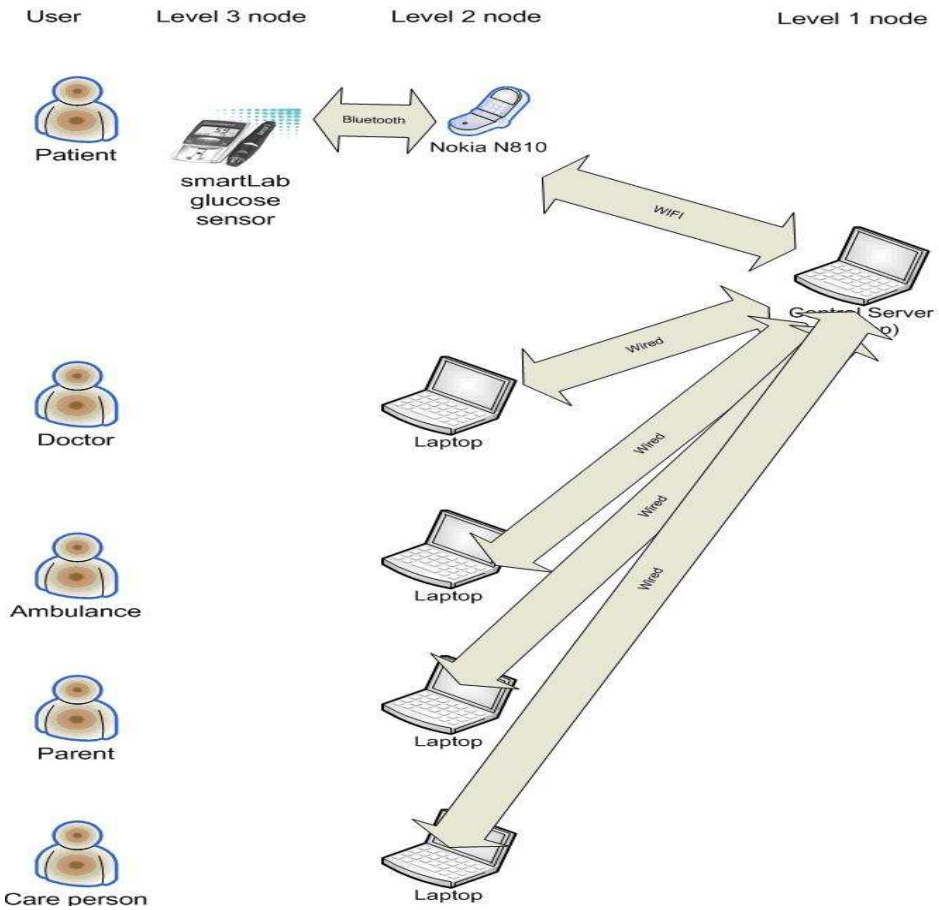
***MORE***

**Network-centric Middleware for group communications and resource sharing across heterogeneous embedded systems**

MORE is a research project currently being undertaken by the Telecommunications Software and Systems Group (part of the Waterford Institute of Technology) along with seven other European partners from France, Spain, Germany and Hungary. These partners are from both academic and industrial establishments.

The main goal of MORE is to provide an efficient disease management service for patients with chronic diseases like diabetes, by employing technology to enhance their care through the provision of remote monitoring.

MORE has published an extract and article detailing its work in the Irish Medical Times journal, June 2008

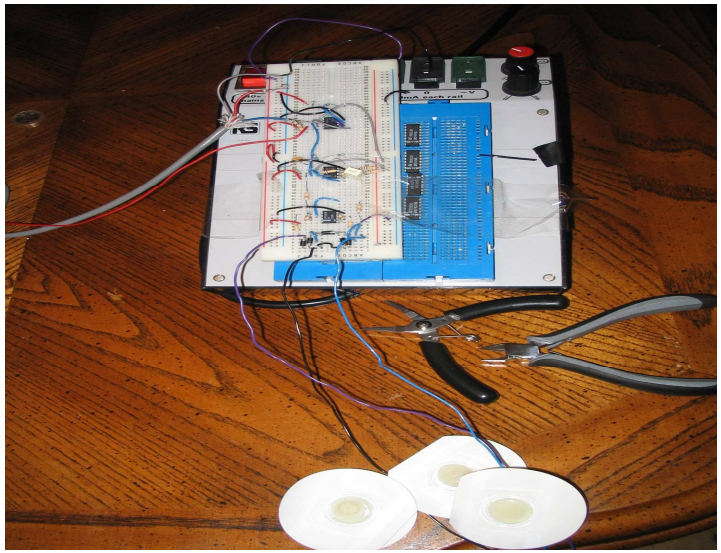



**End user scenario 1:**

MORE is a middleware platform. It is a piece of software that connects two more software applications so that they can communicate effectively.
It will facilitate communication across a group of users as per the diagram.

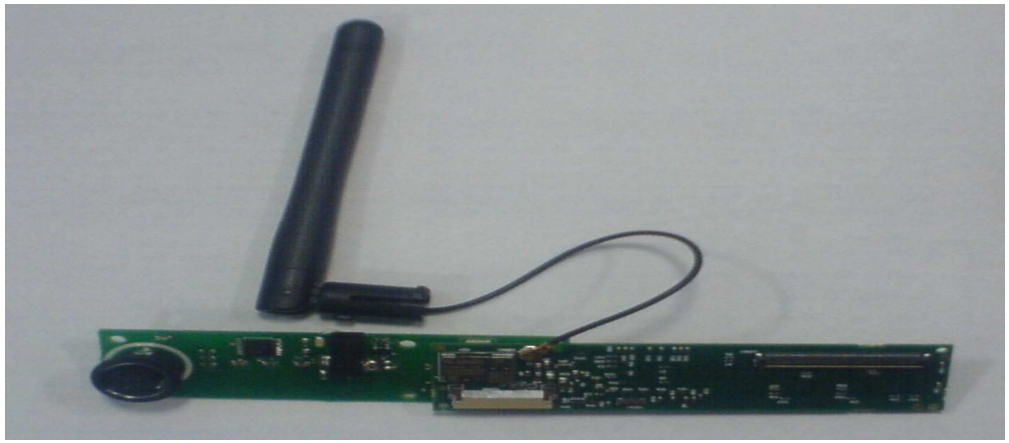
This diagram shows the demonstration setup for the Health Care scenario. The Patient's blood sugar level is being monitored; all the other actors shown on the left are potential members of this patient's care group depending on the readings.

The patient's blood sugar readings are transferred wirelessly from their generic blood sugar monitors to medical personnel via the patient's mobile phone or PDA.



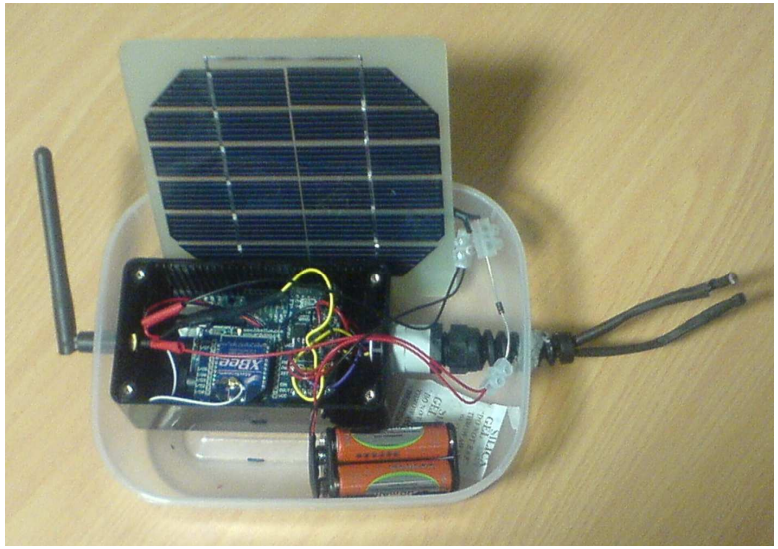
MORE used the Squidbee unit to monitor a person's heart rate by attaching circuitry to it (an ECG). This was achieved by assembling a circuit found on the internet which contained a number of Operational Amplifiers to take in the signals from the electrodes and provide an output for analogue to digital conversion. The circuit also contained several low power resistors, capacitors and diodes for safety.


This is the Blood sugar monitor used in the Health care scenario.



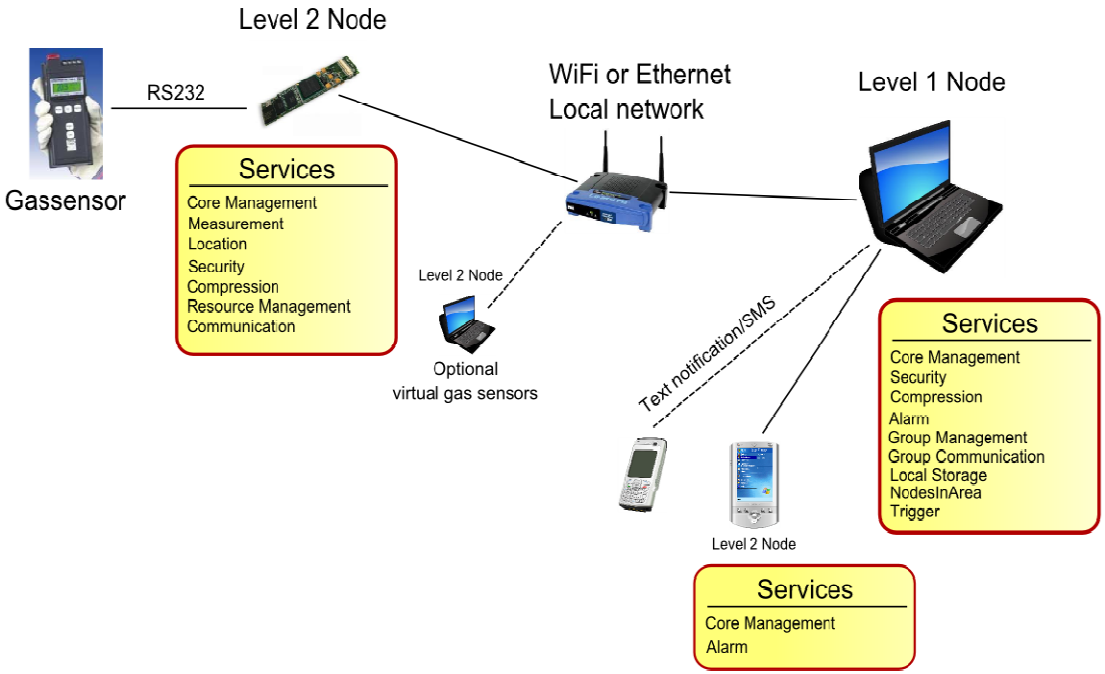
The Gumstix is a fully functional open source computer. It can be individually extended through expansion boards. The MORE prototype platform is based on an XScale PXA270 CPU (ARM 5) with 128MB RAM and 32MB ROM. The Gumstix will serve as a gateway between connected sensors and Web Services. Ethernet or WiFi.

Service developed which extracts sensor data from Squidbee devices (Zigbee enabled)



Squidbee is an Open Hardware and Source wireless sensor device. Twelve digital I/O and six analog I/O allow for the connection of up to 18 sensors. Data collected from these sensors can be securely (the Zigbee module lets you use the AES-128 bit cipher algorithm), wirelessly transmitted using the Zigbee protocol, to a “gateway” which is connected directly to a USB or serial port.

The MORE service developed to interact with the Squidbee unit reads temperature, humidity and, light values from the sensor. For the Squidbee service the MORE group attached circuitry to one of the Squidbee’s six analogue inputs to measure the power level of the attached battery. This reading was then transmitted and corresponding code alerted the user as to when the battery was failing.




**End user scenario 2:**

In order to mitigate and manage environmental damage (e.g. water quality (see EU Water Framework Directive), soil functionality (see EU Soil Protection Policy)) information must be transferred from automatic monitoring facilities (e.g. EU Level-I/II plots) to a heterogeneous group of (a) affected land owners and (b) persons in charge at different administration, research, and management organisations.

The MORE middleware will enable professional users (administrations, research stations, management organisations) to receive and work with maps, e.g. with the help of a smart phone, PDA or MDA in this scenario. Private users (land owners) can receive information in a simplified form, which can be transferred to normal telecommunication instruments (mobile phone, Fax, etc.). Thus, users on different communication levels can be informed effectively and rapidly on probable hot spots (storm damage, critical release of harmful substances into drinking water).

This slide shows the demonstration setup for the Mitigation management scenario.

Mitigation management of environmental damage in the forestry domain.


The EU Partners involved in MORE.

**Project Partners**

1 PRO DV, **Germany**

2 Thales Communications S.A., **France**

3 University of Dortmund, Communication Networks Institute & Embedded Systems Group, **Germany**

4 Applied Logic Laboratory, **Hungary**

5 Waterford Institute of Technology, Telecommunications Software & System Group, **Ireland**

6 Technical University of Dresden, **Germany**

7 University of Debrecen, **Hungary**

8 Universidad Politécnica de Madrid, **Spain**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**PARTNER NAME: INNOVA SPA**

**CONTACT PERSON: FRANCESCO NIGLIA**

**GOOD PRACTICE NAME: HYDRA TECHNOLOGY FOR HOME AUTOMATION**

**SOURCE OF THE GOOD PRACTICE: HYDRA FP6-IP PROJECT**

**TARGET GROUP: AGRO-FOOD, DOP CHEESE PRODUCERS**

**DATE: 11/09/2009**

Grant Agreement: 225004

# Development of a technology for Home Automation and Embedded Devices SMEs sector

We will describe in detail the process that brought an innovative development technology to an SMEs cluster, thus to provide more tools and possibilities to improve their business and their economic sustainability.

# Context: the players

- **Field Associations**: ASSODOMOTICA, EHSA (European Home System Association)
- **SMEs**: domotic and home automation sector
  - In Italy the domotic sector has 200 producers and annual turnover of € 60.000.000 [source : Assodomotica 2009, http://www.assodomotica.it/]
- **Technologies owners**: Research Centres, Industries, technology developers, producers, suppliers (dealer, retailer, installer), consulting engineers, universities.

The analysed SMEs cluster belongs to the Buildings Automation field and Smart Homes, located in the north of Italy.

The process has been also supported by field producers (EHSA) and local associations (ASSODOMOTICA).

It's worth to mentioning the presence of at least an R&D partner, mandatory to have an effective production innovation.

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# Context: T-Connect S.r.l.

**Main Interest:**

- Realisation of applications in the mobile and wireless communication world.
- Identification of the research trends and how merge this directions with the actual market demand.
- Well know and newest wireless technology like:
  - Wi-Fi
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Grant Agreement: 225004

# Context: T-Connect needs analysis

- **Benefit** from the results of any research conducted during the project about WLAN, Bluetooth and ZigBee.
- **Enlarge** its interest in research fields like :
  - Smart Home
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  - Agriculture
- **Expand** its market share.

How we started: survey of T-Connect needs through a technological audit and an explanation of the develop process.

As the develop is one of the most important surveyed issues, we also carried out a SWOT analysis of the applicability and effects of the Middleware within the business of the SME.

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# Context: partner search

- **Technology offer scouting:**
  - **Sector:** Buildings Automation.
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  - Co-funded by associations, public administrations, private companies (Innova, T-Connect S.r.l., The Fraunhofer Institute for Applied Information Technology, University of Reading, Siemens Business Services).
- **Why T-Connect?**
  - Because its particular expertise on mobile and wireless technologies.

Step Two: associate all partner as support company to increase know-how of the project itself. It's worth to mentioning the relevant presence of T-Connect, thanks to its expertise on main topics.

Grant Agreement: 225004

# Context: the HYDRA project

- **Objective:** The HYDRA project aims to alleviate the problems that European industries are facing by researching and developing middleware for networked embedded systems that allows programmers to develop cost-effective, high-performance Ambient Intelligence (AmI) applications using heterogeneous physical devices.
- **Application Areas**: Building Automation, Healthcare, Agricolture.
- Co-funded by the **European Commission** within the FP6–IP [2006-2010].

HYDRA

Follow the description of HYDRA project and its main capabilities to improve the develop of a Middleware for networked embedded system.

The process has been extended to three main Application Areas: Building Automation, Healthcare, Agricolture.

Grant Agreement: 225004

# Context: the objectives of HYDRA

- **Support** of SMEs competitive growth through the adoption of the HYDRA tools (SDK, DDK, IDE) and the development of a middleware based on the Service-oriented architecture paradigm.
- **Support** for reflective properties of components of the middleware.
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# Context: beneficiary SMEs cluster

- **SMEs target group:**
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A description of the mean class representative of the cluster. The action has been tailored on a SME having this profile but it's easily extendible and adoptable by other profiles.

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- **Definition** of the projects to be developed in the analysed context and to be applied in the surveyed cluster starting from "Eu-Domain" predecessor project.
- **Pilot applications: :** One of the first tasks in HYDRA project was creating scenarios of end-user behaviour and interaction with platform functionality in three different user domains, which were selected for pilot applications within the project – Building automation, Healthcare, and Agriculture. These applications are **chosen for** sustainability of the implementation, costs, benefits, range of interested and potentially involved companies.

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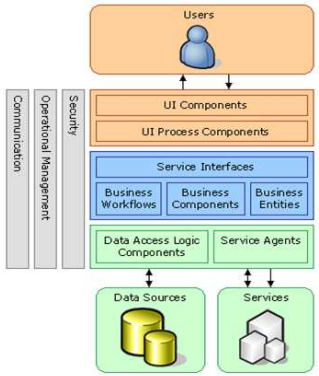
# Technology Develop: technology 1/2

**SOA:** Service Oriented Architecture relatively new fronter for information management.

The key lies in the absence of SOA business logic on the client which is totally agnostic to the platform of implementation, about the protocols, the binding, the type of data, policies with which the service will produce the information requested Service Level Agreement ( SLA).




The technology chosen for the Middleware developing. The SOA technology.

# Technology Develop: technology 2/2

- **Open standards:** to operate in multi-platform environments is necessary or at least advisable, to use only open standards such as XML, WSDL and WS-Security (WSS).
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How to apply the technology to the buildings automation sector, the less invasive solution was the one represented.

# Technology Develop: final idea

- **Develop** a middleware that allows developers to incorporate heterogeneous physical devices into their applications by offering easy-to-use web service interfaces for controlling any type of physical device irrespective of its network technology such as Bluetooth, RF, ZigBee, RFID, WiFi, etc. HYDRA incorporates means for Device and Service Discovery, Semantic Model Driven Architecture, P2P communication, and Diagnostics. Hydra enabled devices and services can be secure and trustworthy through distributed security and social trust components of the middleware.
- **Apply** this technology to each case of Buildings Automation.

Description of the final idea: develop a framework that interacts with other physical devices. This Middleware allow developers to create applications offering easy-to-use web service interface.

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From the T-Connect side, this system gives a very-high added value on the whole develop phase.

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# T-Connect in HYDRA

**Devices and performances analysis**

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**Software development**

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The description lists of the two main sector with which T-Connect works in HYDRA:

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- All the information and studies performed in **HYDRA Project** foster **T-Connect** to follow the ICT research horizontal markets penetration.
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The platform is useful to provide support to ubiquitous intelligence and to stimulate other applications domains to start.


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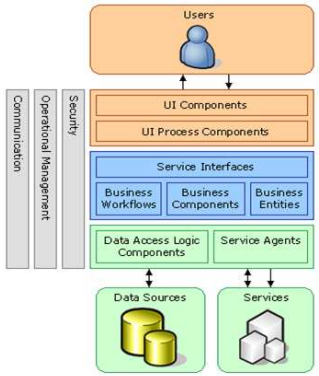


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**PROJECT ACRONYM: NET-SHARE**

**PROJECT FULL TITLE: NETWORK OF ICT EXPERIENCED ORGANIZATIONS, SHARING EXPERIENCES, KNOWLEDGE AND SUPPORTING SME'S.**

**INSTRUMENT: ICT PSP**

**DURATION: 36 MONTHS**

**DISSEMINATION LEVEL: PUBLIC**

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**GOOD PRACTICE NAME: TRENDS AND APPLICATIONS OF EMBEDDED SYSTEMS IN SPAIN**

**SOURCE OF THE GOOD PRACTICE: OPTI SPAIN**

**TARGET GROUP: SMES**

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# Trends and applications of embedded systems in Spain

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# Scope

This report is the result of a prospective study carried by Fundació Ascamm for Fundación OPTI in Spain. The methodology followed consisted in the preparation of a questionnaire by a panel of experts, this questionnaire contained a series of hypothesis (112) about the future evolution of embedded systems. These were sent to 230 Spanish experts from the Administration, Universities, Companies and Public and Private Research Centers.
The questionnaire was answered by 69 experts and included the following subjects:

**Applications**
- Means of transport
- Health
- Industrial Automatization
- Services and Public Infrastructure
- Energy
- Consumer goods
- Environment
- Defense

**Technologies**
- Design and architecture
- Connectivity and Middleware
- Methods, Tools and Processes for systems design

Results are presented as a set of recommendations and trends.

# Results

## 1 -Technologies

### 1.1 - Design and architecture

- **Reliability**, understood as the ability of a system to perform and maintain its functions in routine circumstances, as well as hostile or unexpected circumstances, is ranked as highly important attribute.

- As a consequence the introduction of **specific training in Embedded Systems and Reliability** in Education Plans is also seen as necessary.

- The adoption of **certificates** is also seen as a trend in all kinds of applications.

- From an European level the introduction of **standardized architectures** is identified as highly important. Initiatives such as ARTEMIS, working on the creation of reference architectures for every industry, is pointed as a model.

- A change in **business models** is seen as highly necessary, treating embedded systems not as something monolithic but as the integration of different components.

# Results

## 1 -Technologies

### 1.2 – Connectivity and Middleware

- Enhance the study and developments of **energy aspects** of embedded systems.

- **Automatic and optimized systems communication**: Ad-hoc networks (MESH) will integrate automatically with existing networks, web-services will allow the exchange of data. Systems will show ABC (Allways Best Connected) capabilities.

- Security and protection of data will be ensured through the adoption of **communication protocols**. Identification systems will allow secure and private communication between any two devices.

# Results

## 1 -Technologies

### 1.3 – Methods, Tools and Processes for systems design

- New architectures will allow **easy integration and interoperability** between methods and tools in any ambit.
- Enhance the use of **standard interfaces.**
- Support initiatives that promote the use of **open platforms** (Open Embedded).
- **Validation and certification** processes will be critical for the viability of projects.
- **Specific training** on these subjects.

# Results

## 2 -Applications

### 2.1 – Means of transport

- **Automotive: . X-by-Wire** systems will replace traditional mechanical/hydraulic links.
  **.** Embedded systems will allow **safe autonomous driving**.
  **. Multimedia services** will help to optimize **road efficiency**.
  **. Open architectures** will play a very important role (**AUTOSAR**)
  **. Power electronics**.

- **Rail: .** Introduction of ERTMS will allow **sharing of infrastructures and dynamic rail control.**
  **.** Embedded systems will allow **safe autonomous driving.**

- **Aerospace: .** Embedded systems will allow the implantation of **interactive global air traffic control systems**, improving safety and capacity.
  **. New services for passangers** will be common**:** phone, internet…
  **. Open hardware and software** for commercial use will improve flight safety.

- **Standarization** will allow easy coupling between different modules.

# Results

## 2 -Applications

### 2.2 – Health

- Spanish health system needs to **improve its infrastructure** to be able to take advantage of future developments. Major developments may start in the private sector.
- Devices need to comply with **safety standards** and pass **strict certificates**.
- **Standardization** will be key to ensure interoperability between devices.
- **Enhancement of multidisciplinary teams** to breach the gap between the Health sector and IT sector.
- Collaborate with **microtechnology and nanotechnology** teams to facilitate the miniaturization of embedded systems (implantable devices, surgey…)
- The **Administration should play a sponsor role** to share the costs with companies.

# Results

## 2 -Applications

### 2.3 Industrial Automatization

- **Stock management and logistics** will make use of embedded systems in the products and transportations systems of companies. **Traceability** will also be improved.

- **Maintenance and control of large production systems** will benefit from **sensorized embedded systems.**

- Enhancement of **flexibility and autoconfiguration** of production systems.

- **Real time and distance control** of production systems.

- Again, **standardization** is crucial.

# Results

## 2 -Applications

### 2.4 Services and Public Infrastructure

- Electricity, water and gas meters will be **automatically and remotely read.**
- Embedded systems will be present in **public lightning** to improve their energy efficiency.
- Traffic signs and **infrastructures will communicate with vehicles and traffic control centers**, improving safety and traffic management.
- **Biometric security mechanisms** will be integrated in business processes and transactions.
- The **Administration** needs to get **economically involved** to ensure these trends become a reality.

# Results

## 2 -Applications

### 2.5 Energy

- Embedded systems will allow the **integration and management of distributed generation**.

- Embedded systems will allow to **manage demand** and select the source of energy according to quality and economic criteria.

- **Wireless technologies** will play an important role in the control and maintenance of the energy grid.

# Results

## 2 -Applications

### 2.6 Consumer goods

- Safety and quality of consumer goods will be achieved through **total traceability** of products. This will be possible thanks to embedded systems in intermediate production stages.

- **RFID systems** will play an important role in product traceability.

- Embedded systems will allow **new products and business models** around the ***infotainment*** concept: users will be simultaneously consumers and producers of information.

# Results

## 2 -Applications

### 2.7 Environment

- Sensing embedded systems will be **physically present in the environment** allowing to measure multiple variables in water, air, ground…

- These systems will allow to remotely **monitor and alert of environmental risks in real time.**

# Conclusions

- Enhancement of **collaborations between technological platforms**. **PROMETEO** could be a promoter and coordinator of this initiative.
- Monitor and align with **European platforms (ARTRMIS, ENIAC).**
- Embedded systems should be considered as a **vertical industry**. Solutions should be **exchangeable between different ambits**.
- Introduction of **University training on embedded systems**.
- The administration should support the adoption of embedded systems and regulate a **certification system**.
- **Standardization is essential**. **Companies should participate** in the process of setting standards.